DATABOOK

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the Logical Alternative

HOW TO USE THIS DATABOOK

This databook is organized in sections progressing from overview to detail. However, it is not necessary that it be used in this manner. If you are already familiar with Altera EPLDs and the associated design support versus other semicustom logic alternatives, you can go right to the product data in Section 2. On the other hand, if you're venturing into EPLDs or semicustom logic for the first time, you may choose to acquaint yourself with Section 1 which includes some brief history and a discussion of the technology issues and alternatives in the application specific market.

To place an order, go directly to the Appendices in Section 4 for ordering information, package outlines, or distributor locations.

If this databook doesn't answer your technical questions, please call our applications HOT-LINE (408) 984-2805 extension 102, and we will help you directly.

INTRODUCTION TO ALTERA **PAGE NO.**

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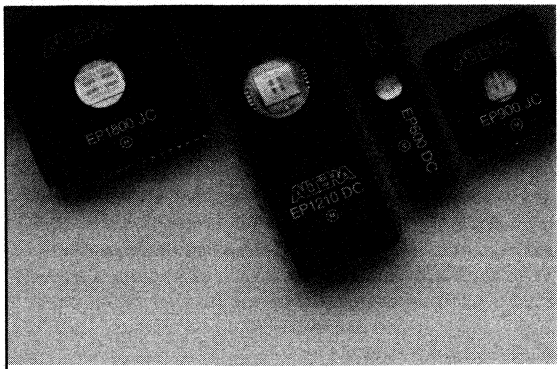
ALPHA-NUMERIC INDEX



ALTERA CORPORATON

Altera Corporation was founded in 1983 to provide an alternative solution to custom masked gate arrays for the design of application specific, VLSI density logic functions. The founders of Altera believed that the problems of high development costs, long lead times, lack of design iteration flexibility and dedicated inventory could be eliminated through the use of standard, user configurable (or programmable) components.

USER CONFIGURABLE INTEGRATED CIRCUITS (UCIC)

By combining CMOS and EPROM erasable cell technologies Altera created the industry's first Erasable Programmable Logic Device (EPLD) in 1984. This has led to the introduction of a full family of EPLDs spanning the range from 300 to over 2000 gates. These products provide a convenient, low cost means of integrating dozens of TTL and CMOS SSI/MSI devices into a handful of packages. EPLDs represent the first of many planned families of User Configurable Integrated Circuits, UCICs, from Altera. Products will include devices aimed at specific system functions, such as state machines and microprocessor peripherals as well as very high density, general purpose logic integration.

UCIC DEVELOPMENT TOOLS

A critical factor in the rapid, world wide acceptance of Altera's user configurable ICs has been the availability of low cost, easy to use software and hardware development tools. Available on both IBM PC compatible and DEC VAX computer platforms, Altera's tools provide everything required to design, debug and program custom logic functions in the user's facility.

At the heart of these software tools is A+PLUS, Altera's proprietary logic compiler. A+PLUS contains a powerful fitter, which provides the EPLD equivalent to automatic place and route capability. A variety of design entry methods is offered including state machine and schematic capture using high level TTL macrofunction building blocks as well as primitive gate elements. Simulation and interface programs to third party CAE products are also available.

PHILOSOPHY AND DIRECTION

Altera believes that these development tools are a critical factor for the advancement of user configurable semiconductor technology. In order that component utility and ultimately designer efficiency be maximized, the semiconductor device and the software must be developed in parallel and concert. If one is subordinated to the other, the total product combination will suffer. In line with this belief, Altera has invested in approximately equal sized R&D staffs in the areas of Software Development and Integrated Circuit Design.

One benefit of this approach is that when Altera introduces a new product to the market place, software and hardware support are in place on the day of introduction. This level of support and service is unique in the industry.

Altera also works closely with the leading third party vendors to assure its customers the availability of appropriate tools for the production environment.

Altera, as a company, is focused entirely on the application of CMOS erasable technology to the user configurable integrated circuit market. By focusing exclusively on these products, Altera has been able to achieve superior quality in devices, tools and services. It is the Company's intent to retain its position as the technology and market leader in this area.

Altera's products are sold by manufacturers representatives and major electronic distributors throughout the world. Intel Corporation and others are licensed second sources for many of the Altera products described in this catalog.

THE USER CONFIGURABLE INTEGRATED CIRCUIT (UCIC) CONCEPT

To achieve improved system performance in the marketplace, more and more manufacturers have sought higher levels of integration (functional density) for the electronic components in their products. This has led to various forms of custom chips that require lengthy development lead times and sizable design costs. The concept of User Configurable Integrated Circuits, UCICs, is to provide the benefits of large scale integration *without* the drawbacks of custom chips.

A few of the most significant benefits of large scale logic integration are:

- Lower manufacturing costs
- Lower power

- Higher reliability
- Proprietary design protection
- Additional features

As end users of semiconductors moved to higher and higher levels of integration chip designers found it increasingly difficult to define larger and larger common "building blocks" of logic. These difficulties led to the emergence of the *user-defined* Application-Specific Integrated Circuit (ASIC), sometimes more accurately described as User Specific (USIC) or Customer Specific (CSIC) devices.

The options presently available for customer-specific logic are:

- Full Custom
- Standard Cell Library
- Gate Array
- User Configurable (Programmable)

The first three choices are custom masked and are not wholly satisfactory for system designers and manufacturers due to several problems:

- Development lead times are relatively long, requiring from 6 to 20 weeks for the fastest solution.
- Design costs are significant, varying from $10K to $40K as a minimum.
- Inventory is dedicated which is expensive and prohibits adequate second sourcing.
- Semiconductor distributors have difficulty participating in this business—thus limiting widespread use.
- None of these solutions address the fundamental issue that engineering is inherently an interactive process. Design changes in midstream are not allowed due to lead time and inventory constraints.

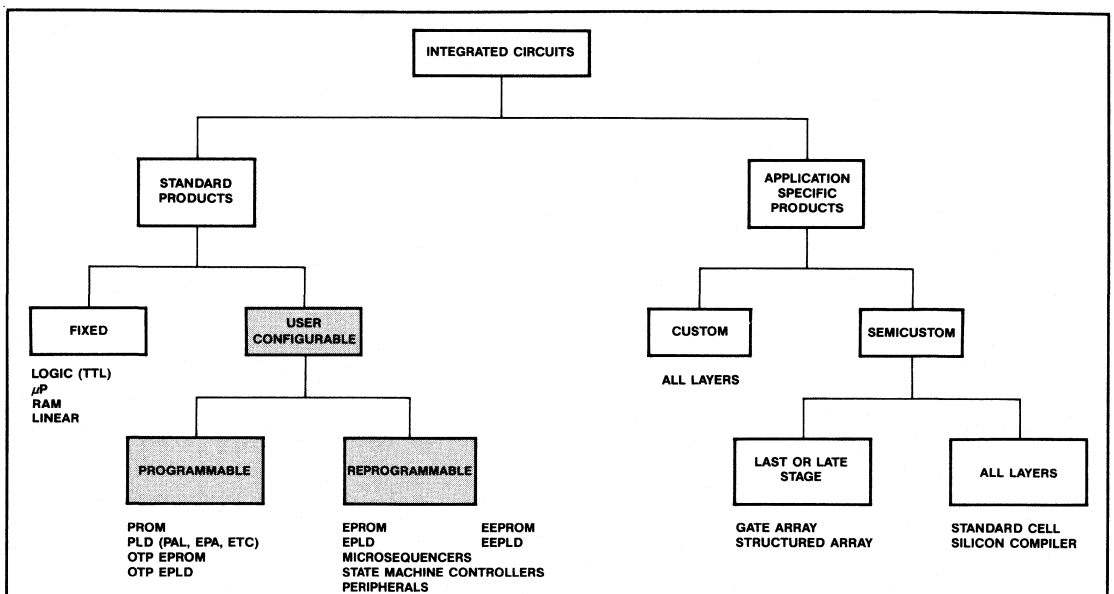
As a result of these restrictions, many designers are still reluctant to switch from standard logic to application-specific logic.

Attempts to eliminate these restrictions have led to an increasing interest in user configurable or programmable logic devices. The concept of user configurable logic is to provide the designer with the benefits of custom LSI chips from standard products. The benefits of such parts include off-the-shelf availability, minimal design costs, multiple sourcing from distributors and manufacturers, and flexible, interchangeable inventory.

BIPOLAR FUSE TECHNOLOGY

In the past all programmable logic products were implemented using bipolar fuse technology. These products eliminated the lead time and development cost penalties of the mask customized solutions previously mentioned, but brought with them their own inherent limitations:

- Bipolar, with its high power dissipation, cannot provide the integration density required.
- Fuse programming does not allow complete testing at the factory and is inefficient in silicon utilization.
- The devices can only be programmed once; therefore, mistakes in development result in scrap, a significant penalty with high density parts.
- The programming software and development tools are primitive and tedious to use.



THE INTEGRATED CIRCUIT FAMILY TREE

CMOS ERASABLE TECHNOLOGY

Altera was the first supplier to overcome these problems of programmable logic when it introduced its EPLD line of user-programmable logic devices incorporating CMOS floating-gate technology.

Altera EPLDs are manufactured with high-speed complementary metal oxide semiconductor (CMOS) technology. Compared to bipolar fuse technology, CMOS provides lower power dissipation and a cooler operating temperature which enables designers to pack a greater number of logic functions onto a chip.

Altera's EPLDs use an EPROM programming mechanism. This technology, used in MOS memories since the early 1970's, brings further advantages. It enables the devices to be reprogrammed in the event of any design changes. The fact that programming can be erased also permits thorough testing during the manufacturing process.

EASY TO USE DESIGN TOOLS

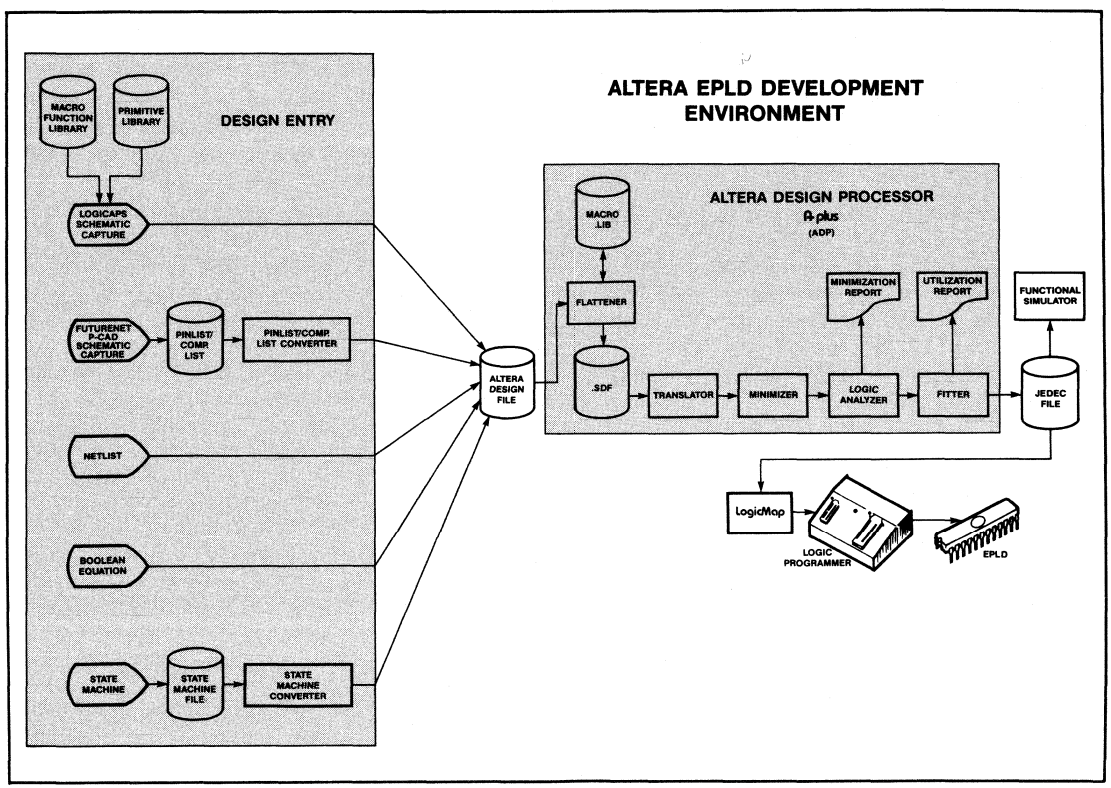
For user-configurable circuits to reach the broad base of existing SSI/MSI TTL users, the programming and design tools must meet three criteria:

- Low cost
- Easy to use
- Personal availability and access.

Today, the most widely available source of computing power is the personal computer. By creating development tools that fit the personal computer environment, all three of these criteria can be met.

As in the area of component architecture, Altera is committed to provide effective, flexible solutions to the CAD/CAE problems the system designer faces. Particularly in those areas which require extensive device-specific knowledge, Altera has developed an effective set of IBM-PC and DEC-VAX/VMS based CAD tools to handle the problems of design entry and programming. This package, known as A+PLUS (Altera Programmable Logic User System) provides a powerful design support tool that matches the continually expanding capabilities of Altera programmable logic devices.

Within A+PLUS, the user may enter a design via high level TTL MacroFunctions or primitive gate symbols using graphic schematic diagrams, text-based netlist entries, state machine descriptions, or Boolean equations. Once the design is entered, Altera's fully automated integration process, called the Altera Design Processor (ADP), translates the design into an industry-standard (JEDEC) PLD programming file. The JEDEC file is used to directly program the target EPLD using Altera-supplied hardware, or general-purpose third party programmers.



FITTING

The translation of a design from its original input format (be it equation, schematic, or other) to a device-specific programming map is typically called fitting. Early PAL device assemblers provided no support for software-assisted logic minimization: the user in essence had to determine the minimal set of equations to implement his logic. This could be quite time consuming and was early-on recognized as a mechanical task well suited to software algorithms.

Altera's ADP package utilizes logic minimization schemes such as DeMorgan's Inversion to aid the designer in minimizing his logic and optimally fitting into a given device. This process becomes more complex as devices become more sophisticated. Variable product term distribution, multiple flip-flop types, local/global feedback all complicate the process as they add capability.

Fitting is a process which is obviously sensitive to device architecture. A very compelling reason for vendor-supplied development tools such as Altera's A+PLUS is the need for close interaction between tools and architecture. Much as optimizing compilers must have knowledge of the target computer architecture, fitters must have knowledge of their devices. Tools developed in parallel with device development will arrive in a timely fashion at device introduction rather than lagging by substantial periods of time.

Altera's answer to the fitting problem is its ADP package. It performs three major functions.

First, regardless of the type of design entry method used, it translates the design into internal logic equations. At this stage, most design syntax errors are detected and reported to the user.

Second, the ADP performs sophisticated Boolean logic reductions on the translated design in order to maximize utilization of the EPLD's resources. The user is given complete control over the application of minimization and inversion techniques.

Finally, the ADP matches requirements of a specific design with the known resources of an Altera part. Automatically, or with user input, the ADP places each logic function in the optimum location and selects the appropriate interconnection paths and device pin assignments.

The actual fitting process results in a utilization report and a JEDEC standard programming file. The utilization report informs the user how the design was implemented and points out any unused resources remaining in the device.

SIMULATION AND TEST CONSIDERATIONS

Design checking before system integration from components has taken on new importance with more complex designs. Granted, with EPLDs the user does have the luxury of relatively painlessly reprogramming his device if an error in the design should be found. However, by employing simulation at an early stage this type of wasted effort can be prevented. Altera offers P.C. based simulation capability.

Most customer specific logic solutions, such as gate arrays and fuse based PLDS, require extensive customer investment in test program development and test equipment. EPLDs eliminate this need to develop specific tests for the unique design programmed into each device. Because it is erasable, each cell can be programmed and tested prior to shipment from the factory. Through this generic testability the I/C manufacturer can guarantee 100% programming yield to ther user.

SUMMARY

Altera, with its EPLD products and development system support tools, has addressed the limitations of gate arrays and fuse programmable logic. The benefits to the system designer are:

- no lead times
- low design costs
- multiple sourcing from distributors and manufacturers
- ease of design changes
- multiple programming, if necessary
- low power dissipation from CMOS technology
- high density products that maximize function, integration, and quality
- maximum flexibility in each chip that comes from programmable architecture, and the ability to erase and reprogram
- a self-contained low-cost sophisticated development system.

EPLDs are now a cost-effective solution to the problem of large scale random logic integration. EPLDs are the simplest form of high density application-specific logic to implement. As such, they will be a key ingredient to boosting electronic engineering productivity over the next decade.

Future EPLD's and new user configurable devices will incorporate new architectures which will allow the rapid design of complex devices with the equivalent of several thousand gates on a single chip. The result will be the integration of complex subsystems on single chips much as large-scale gate arrays permit today.

DEVICE DATASHEETS	PAGE NO.

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DEVICE SELECTOR CHART

EPLD	PACKAGE	PINS	MACRO CELLS (REGISTERS)	BURIED REGISTERS	INPUTS	I/O	fmax MHz	Icc mA	STANDBY Icc mA
EP1800J	JLCC	68	48	16	16	48	20.8	30.0	0.15
EP1800L	PLCC	68	48	16	16	48	20.8	30.0	0.15
EP1800G	PGA	68	48	16	16	48	20.8	30.0	0.15
EP1210D	CerDIP	40	28	4	12	24	26.2	10.0	6.0
EP1210P	OTP DIP	40	28	4	12	24	26.2	10.0	6.0
EP1210J	JLCC	44	28	4	12	24	26.2	10.0	6.0
EP1210L	PLCC	44	28	4	12	24	26.2	10.0	6.0
EPB1400D	CerDIP	40	20	32	8	28	35.0	70.0	70.0
EPB1400P	OTP DIP	40	20	32	8	28	35.0	70.0	70.0
EPB1400J	JLCC	44	20	32	8	28	35.0	70.0	70.0
EPB1400L	PLCC	44	20	32	8	28	35.0	70.0	70.0
EP910D	CerDIP	40	24	—	12	24	50.0	15.0	0.1
EP910P	OTP DIP	40	24	—	12	24	50.0	15.0	0.1
EP910J	JLCC	44	24	—	12	24	50.0	15.0	0.1
EP910L	PLCC	44	24	—	12	24	50.0	15.0	0.1
EP900D	CerDIP	40	24	—	12	24	26.3	15.0	0.15
EP900P	OTP DIP	40	24	—	12	24	26.3	15.0	0.15
EP900J	JLCC	44	24	—	12	24	26.3	15.0	0.15
EP900L	PLCC	44	24	—	12	24	26.3	15.0	0.15
EP610D	CerDIP	24	16	—	4	16	66.7	3.0	0.1
EP610P	OTP DIP	24	16	—	4	16	66.7	3.0	0.1
EP610J	JLCC	28	16	—	4	16	66.7	3.0	0.1
EP610L	PLCC	28	16	—	4	16	66.7	3.0	0.1
EP600D	CerDIP	24	16	—	4	16	26.3	10.0	0.15
EP600P	OTP DIP	24	16	—	4	16	26.3	10.0	0.15
EP600J	JLCC	28	16	—	4	16	26.3	10.0	0.15
EP600L	PLCC	28	16	—	4	16	26.3	10.0	0.15
EPS444D	CerDIP	24	—	—	8	12	30.0	130.0	65.0
EPS444P	OTP DIP	24	—	—	8	12	30.0	130.0	65.0
EPS448D	CerDIP	28	—	—	8	16	30.0	130.0	65.0
EPS448P	OTP DIP	28	—	—	8	16	30.0	130.0	65.0
EPS448J	JLCC	28	—	—	8	16	30.0	130.0	65.0
EPS448L	PLCC	28	—	—	8	16	30.0	130.0	65.0
EP320D	CerDIP	20	8	—	10	8	50.0	50.0	0.15
EP320P	OTP DIP	20	8	—	10	8	50.0	50.0	0.15
EP310D	CerDIP	20	8	—	10	8	35.7	40.0	30.0

Package Abbreviations:

CerDIP = windowed ceramic dual-in-line.
OTP DIP = one-time-programmable plastic dual-in-line.
JLCC = windowed ceramic leaded chip-carrier.
PLCC = one-time-programmable plastic leaded chip-carrier.
PGA = windowed ceramic pin-grid array

note (1) The application areas indicated cover typical circuit areas appropriate for the device shown. The larger scale devices can readily be used in wider application areas than the lower scale integration components.

note (2) The fmax values shown represent the highest speed grade. For detailed performance refer to the individual datasheets within this book.

note (3) Icc and fmax are typical values for EPB1400, EPS448, EPS444, EP910 and EP610.

APPLICATIONS note (1)

	LSI CUSTOM LOGIC	TTL-LOGIC REPLACEMENT	STATE MACHINES	ADDRESS DECODERS	MICRO-CODED CONTROLLERS	MICROPROCESSOR INTERFACE	PAL REPLACEMENT
EP1800J	*	*					
EP1800L	*	*					
EP1800G	*	*					
EP1210D	*	*	*	*		*	
EP1210P	*	*	*	*		*	
EP1210J	*	*	*	*		*	
EP1210L	*	*	*	*		*	
EPB1400D	*	*				*	
EPB1400P	*	*				*	
EPB1400J	*	*				*	
EPB1400L	*	*				*	
EP910D		*	*	*		*	
EP910P		*	*	*		*	
EP910J		*	*	*		*	
EP910L		*	*	*		*	
EP900D		*	*	*		*	
EP900P		*	*	*		*	
EP900J		*	*	*		*	
EP900L		*	*	*		*	
EP610D		*	*	*			*
EP610P		*	*	*			*
EP610J		*	*	*			*
EP610L		*	*	*			*
EP600D		*	*	*			*
EP600P		*	*	*			*
EP600J		*	*	*			*
EP600L		*	*	*			*
EPS444D			*		*		
EPS444P			*		*		
EPS448D			*		*		
EPS448P			*		*		
EPS448J			*		*		
EPS448L			*		*		
EP320D				*			*
EP320P				*			*
EP310D				*			*

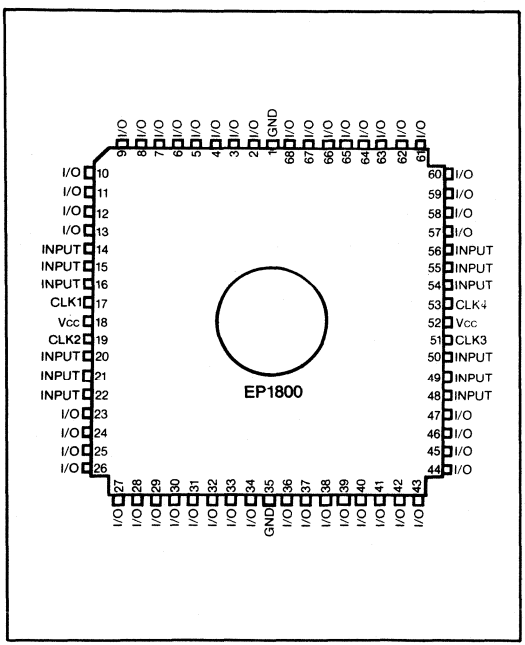
2

48 MACROCELL EPLD — EP1800

FEATURES

- Erasable, User-Configurable LSI circuit capable of implementing 2100 equivalent gates of conventional and custom logic.
- Speed equivalent to 74LS TTL with 20 MHz clock rates.
- "Zero Power" (typically 35 μA standby).
- Active power of 250 mW at 5 MHz.
- Forty-eight Macrocells with configurable I/O architecture allowing 64 inputs or 48 outputs.
- Programmable clock option allows independent clocking of all registers.
- Accepts popular TTL SSI and MSI based MacroFunction design inputs.
- TTL/CMOS I/O compatibility.
- 100% generically testable—provides 100% programming yield.
- Full military capability.
- CAD support from Altera's A+PLUS Development System featuring schematic capture design entry with extensive Primitive and MacroFunction libraries.
- Packaged in a 68 pin ceramic (window) and plastic (one-time programmable) JLCC, PLCC, and PGA configurations.

CONNECTION DIAGRAM



GENERAL DESCRIPTION

The EP1800 series of CMOS EPLDs from Altera offer LSI density, TTL equivalent speed performance and low power consumption. Each device is capable of implementing over 2100 equivalent gates of SSI, MSI and custom logic circuits. The EP1800 series is packaged a 68 pin J-Leaded Chip Carrier and Pin Grid Array, available in ceramic (erasable) and plastic (one-time-programmable) versions.

The EP1800 series is designed as an LSI replacement for traditional Low Power Schottky TTL logic circuits. Its speed and density also make it suitable for high performance complex functions such as dedicated peripheral controllers and intelligent support chips. IC count and power requirements can be reduced by several orders of magnitude allowing similar reduction in total size and cost of the system, with significantly enhanced reliability.

The EP1800 architecture has been configured to facilitate design with conventional TTL SSI and MSI building blocks as well as simple, optimized gate and flip-flop elements. Schematic descriptions of these functions are stored in a library. The desired TTL logic functions are selected and interconnected "on-screen" with a low cost, personal computer based, workstation. The Design Processor within Altera's A+PLUS Development System then automatically places the functions in appropriate locations within the EPLD's internal structure. Also included in the Development System is EPLD programming hardware and software. A+PLUS is available for the IBM Personal Computer (and compatibles).

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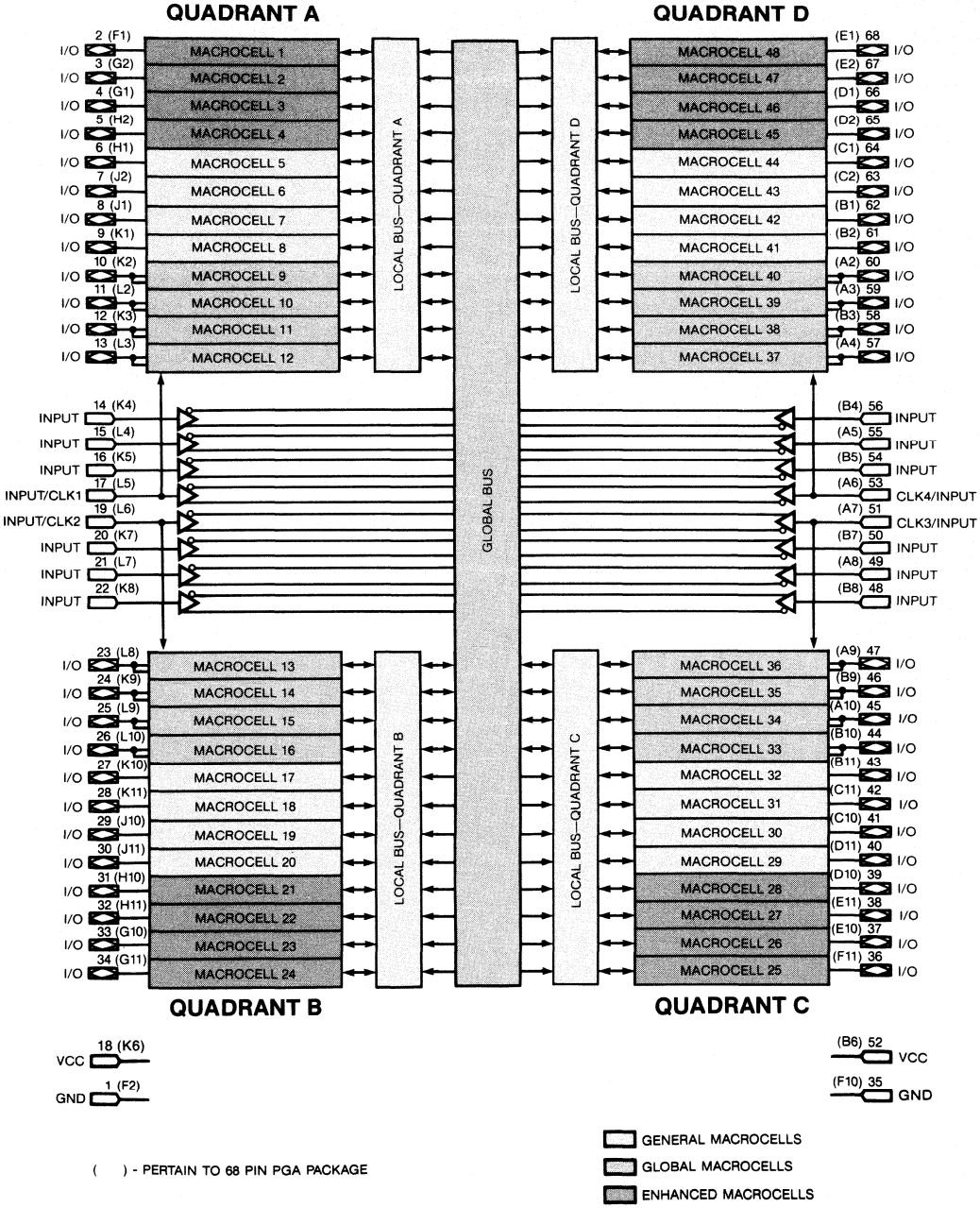
FIG. 1 EP1800 BLOCK DIAGRAM



The EP1800 uses a sub-2 micron CHMOS EPROM technology employing EPROM transistors to configure logic connections. User defined logic functions are constructed by selectively programming EPROM cells within the device. The EPROM technology also allows 100% generic testing (all devices are 100% tested at the factory). The devices can be erased with ultraviolet light. Design changes are no longer costly or time consuming, nor is there the need for post-programming testing.

FUNCTIONAL DESCRIPTION

The EP1800 series of Erasable Programmable Logic Devices (EPLDs) use CMOS EPROM cells to configure logic functions within the device. The EP1800 architecture is 100% user configurable, allowing the device to accommodate a variety of independent logic functions.

The Block Diagram is shown in Fig. 1. Externally, the EP1800 provides 16 dedicated data inputs, 4 of which may be used as system clock inputs. There are 48 I/O pins which may be individually configured for input, output, or bi-directional data flow.

MACROCELLS

Internally, the EP1800 architecture consists of a series of Macrocells. All logic is implemented within these cells. Each Macrocell, shown in Fig. 2A, contains three basic elements: a Logic Array, a selectable register element, and a tri-state I/O buffer. All combinatorial logic such as Exclusive-OR, NAND, NOR, AND, OR and Invert gates are implemented within the Logic Array. For register applications each Macrocell provides one of 4 possible flip-flop options; D, T, JK, SR. Each EP1800 Macrocell is equivalent to over 40 2-input NAND gates.

The EP1800 is partitioned into four identical quadrants. Each quadrant contains 12 Macrocells. Input signals into the Macrocells come from the EP1800 internal bus structures. Macrocell outputs may drive the EP1800 external pins as well as the internal buses. Fig. 2B illustrates a simple logic function that can be implemented within a single Macrocell. Note that all combinatorial logic is implemented within the Logic Array, a JK flip-flop is selected, and the tri-state buffer is permanently enabled.

Sixteen of the EP1800's 48 Macrocells offer increased speed performance through the Logic Array. These "Enhanced Macrocells" can be utilized for critical

FIG. 2A MACROCELL COMPONENTS

Each 1800 Macrocell consists of 3 basic components:
(1) A logic array for gated logic. (2) a flip-flop for data storage (selectable options include D, T, JK, SR). The flip-flop may be bypassed for purely combinatorial functions. (3) A tri-state I/O buffer to define input, output or bi-directional data flow.

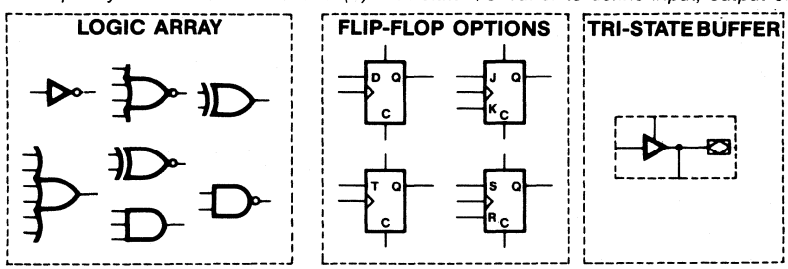
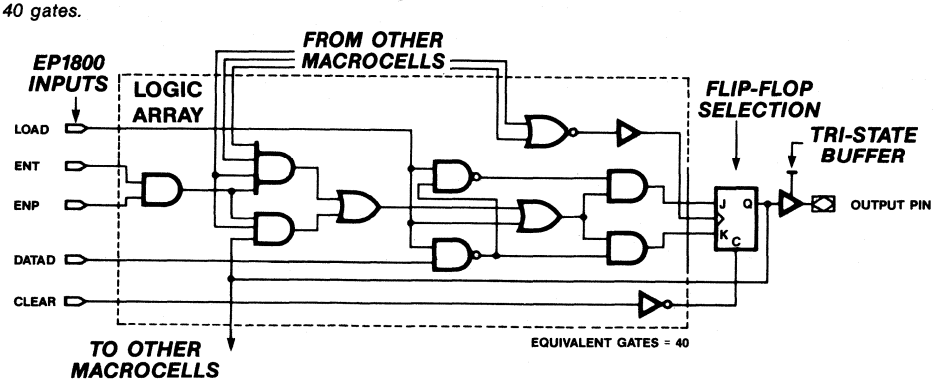


FIG. 2B SAMPLE CIRCUIT

Typical logic functional implemented into a single Macrocell. Each EP1800 Macrocell can accommodate the equivalent of 40 gates.



combinatorial logic delay paths. There are four enhanced Macrocells for each EP1800 quadrant, see Figure 1. The AC Characteristics show Logic Array delay times for enhanced and general Macrocells.

Another 16 Macrocells provide dual functions. These "Global Macrocells", see Figure 1, allow the Macrocell to implement buried logic functions and, at the same time, serve as dedicated input pins. Thus, the EP1800 may have an additional 16 input pins giving a total of 32 inputs. The global Macrocells have the same timing characteristics as the general Macrocells.

CLOCK OPTIONS

Each of the EP1800 internal flip-flops may be clocked independently or in user defined groups. Any input or internal logic function may be used as a clock. These clock signals are activated by driving the flip-flop clock input with a clock buffer (CLKB) primitive. In this mode, the flip-flops can be configured for positive or negative edge triggered operation.

Four dedicated system clocks (CLK1-CLK4) also provide clock signals to the flip-flops. System clocks are connected directly from the EP1800 external pins. With this direct connection, system clocks give enhanced clock to output delay times than internally generated clock signals. There is one system clock per EP1800 quadrant. When using system clocks, the flip-flops are positive edge triggered (data transitions occur on the rising edge of the clock).

MACROFUNCTIONS

MacroFunctions, shown in Fig. 3, allow the circuit designer to use popular TTL SSI and MSI building blocks. Many MacroFunctions are standard TTL circuits such as counters, comparators, multiplexers, decoders, shift registers, etc. and are identified by their familiar TTL part numbers. MacroFunctions are constructed by combining one or more Macrocells. These high-level function blocks may be combined with low-level gate and flipflop elements to produce a complete logic design.

An automatic function built into the A+PLUS CAD software ensures that the use of MacroFunctions causes no loss of design efficiency. A+PLUS analyzes the complete logic schematic and automatically removes unused gates and flip-flops from any MacroFunction employed. This "MacroMunching" process allows the logic designer to employ MacroFunctions without the headaches of optimizing their use.

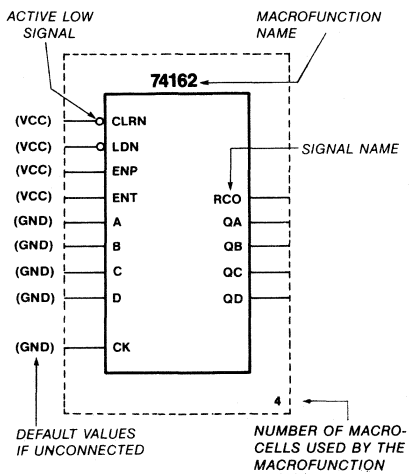
All inputs to MacroFunctions are designed with "intelligent" default input signal levels (VCC or GND). Normally active high and low signals or unused inputs can simply be left unconnected . . . further improving productivity and reducing the burden placed on the designer.

DESIGN LIBRARIES

Altera provides both a Primitive and MacroFunction library. These libraries are used with Altera's LogiCaps schematic capture design entry to specify the logic. Elements from both libraries may be used in the same design, allowing full utilization of the EP1800 resources. The Primitive library is included with LogiCaps software package. The MacroFunction library, PLSLIB-TTL, is available as an option.

FIG. 3 MACROFUNCTION SYMBOL

MacroFunctions are TTL compatible SSI and MSI circuits giving the circuit designer a high-level approach to EPLD design. MacroFunctions include input default values to unconnected inputs and "MacroMunching" to unused outputs. Altera's MacroFunction library consists of over 100 components.



74162 FUNCTION TABLE

INPUTS									OUTPUTS				
CK	LDN	CLRN	ENP	ENT	D	C	B	A	Q_D	Q_C	Q_B	Q_A	RCO
↑	X	L	X	X					L	L	L	L	L
↑	L	H	X	X	d	c	b	a	d	c	b	a	L
↑	H	H	X	L					HOLD COUNT				L
↑	H	H	L	X					HOLD COUNT				L
↑	H	H	H	H					COUNT UP				L
↑	H	H	H	H					H	L	L	H	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
↑ = transition from low to high level
a,b,c,d = level of steady state input at inputs A,B,C,D

PRIMITIVE LIBRARY

The Primitive library consists of 80 low-level logic gates, flip-flop, and I/O symbols. See PLE40 data sheet. Basic gates provided are AND, OR, NAND, NOR, Exclusive OR and NOR, and NOT functions. De-Morgan's inversion (bubble input) of each gate is also included. These logic gates have a maximum of 12 inputs. Larger gates may be constructed by chaining primitives together. Flip-flops in the form of D, T, JK, and SR types are supplied. Each flip-flop has asynchronous clear capability. To connect signals to external pins, input and tri-state I/O buffers are available. For the designer's convenience, "compound primitives" which combine register and I/O buffers are also supplied.

MACROFUNCTION LIBRARY

Altera's MacroFunction library encompasses over 100 high-level building blocks that can greatly increase design productivity. See PLSLIB-TTL data sheet. The library contains the most commonly used TTL SSI and MSI functions. In addition, a number of more specialized MacroFunctions have been added. These blocks perform logic functions in an optimum manner for EPLD implementation. They include counters implemented with toggle flip-flops, inhibit gates, combinational shift-registers/counters and a variety of useful logic structures not found in standard TTL devices.

STARTING A DESIGN

To get started on an EP1800 design the following sequence of preliminary steps is suggested. The equations given will help estimate how to build your system with EP1800's.

FIG. 4 LOCAL MACROCELL LOGIC ARRAY

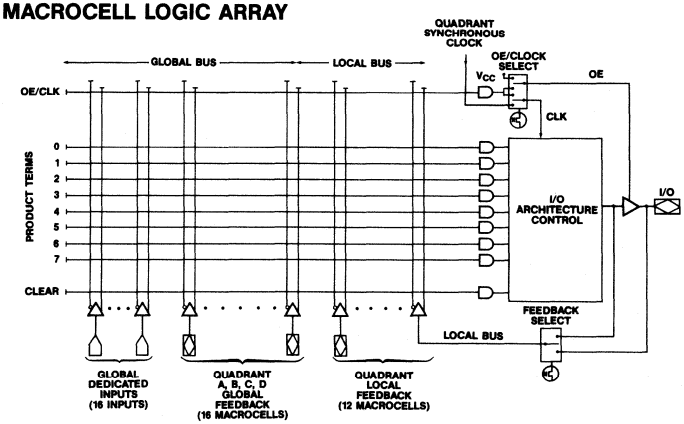
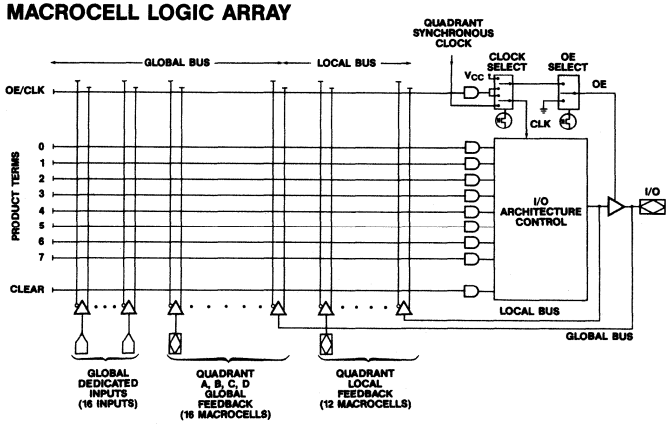


FIG. 5 GLOBAL MACROCELL LOGIC ARRAY



PARTITIONING

First, partition the complete system into functional blocks. Major functional blocks may be expressed in standard MSI TTL form for integration within the EP1800. Should the design require a multiple EPLD solution, the I/O connections which interface between the EPLDs should be minimized. The complete schematic should be structured as a set of subsystems such as counters, shift-registers, comparators, etc., to allow easy design entry.

TIMING SPECIFICATIONS

Knowledge of the base clock frequency and critical timing paths are necessary to make the correct choice of EPLDs. The EP1800 series can support circuits operating up to 25 MHz. Critical timing paths are determined based upon input buffer, logic array, and output buffer delays. (Refer to AC characteristics). Smaller EPLDs, such as the EP900 or EP600, can be used for circuitry that demand higher speed requirements on critical paths.

ESTIMATING A FIT

To estimate the amount of logic which will fit into an EP1800, the number of input and output pins, and the number of Macrocells must be specified.

To estimate the number of Macrocells, determine; (a) the number of buried flip-flops (flip-flops which do not drive output pins), and (b) the number of Macrocells used by MacroFunctions. Since basic gates are implemented within the Logic Array, in most instances they do not require an entire Macrocell, thus they may be safely ignored in the estimation.

Each member of the MacroFunction library has a maximum number of Macrocells used to build the function. This number is shown in the lower right hand corner of the symbol. Refer to the PLSLIB-TTL datasheet to determine how many Macrocells each MacroFunction requires. Note that some MacroFunctions have no Macrocell specification. These functions use only a portion of the logic array, thus other logic could be added before the entire Macrocell is used.

Estimation Formula:

(a) Determine the number of output pins = OP
(b) Determine the number of input pins = IP
where IP = number of inputs -16
(if less than zero, enter zero)
(c) Determine the number of Macrocells = BFF + MR
where BFF = Buried Flip-Flops
and MR = MacroFunction Requirements

If OP + IP + BFF + MR $<$ 48 the design will most likely fit into an EP1800. Complete the design using Altera's LogiCaps and A+PLUS CAD tools.

DESIGN SECURITY

The EP1800 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

FIG. 6 I_{CC} VS F_{MAX}

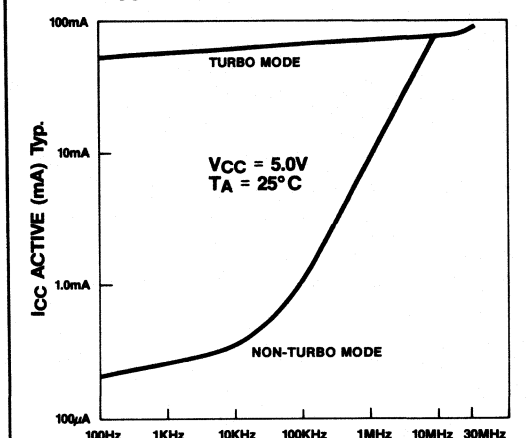
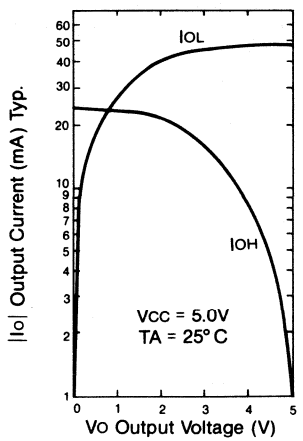


FIG. 7 OUTPUT DRIVE CURRENTS



ABSOLUTE MAXIMUM RATINGS

Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	With respect to GND note (3)	-2.0	7.0	V
V_{PP}	Programming supply voltage		-2.0	13.5	V
V_I	DC INPUT voltage		-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		-300	+300	mA
I_{OUT}	DC OUTPUT current, per pin		-25	+25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	-65	+150	°C
T_{AMB}	Ambient temperature	Under bias	-65	+135	°C
ESD	ElectroStatic Discharge Voltage		±2100		V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage	note (6)	4.75 (4.5)	5.25 (5.5)	V
V_I	INPUT voltage		0	V_{CC}	V
V_O	OUTPUT voltage		0	V_{CC}	V
T_A	Operating temperature	For Commercial	0	70	°C
T_A	Operating temperature	For Industrial	-40	85	°C
T_C	Case temperature	For Military	-55	125	°C
T_R	INPUT rise time	note (9)		500	ns
T_F	INPUT fall time	note (9)		500	ns

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)
(V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial)
(V_{CC} = 5V ± 10%, T_C = -55°C to 125°C for Military)*
Note (1) and (6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3		0.8	V
V_{OH}	HIGH level TTL output voltage	I_{OH} = -4mA DC	2.4			V
V_{OH}	HIGH level CMOS output voltage	I_{OH} = -2mA DC	3.84			V
V_{OL}	LOW level output voltage	I_{OL} = 4mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	-10		+10	µA
I_{OZ}	3-state output off-state current	V_O = V_{CC} or GND	-10		+10	µA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND No load		35	150	µA
I_{CC2}	V_{CC} supply current (non-turbo)	V_I = V_{CC} or GND No load, f = 1.0 MHz note (7)		15	30 (40)	mA
I_{CC3}	V_{CC} supply current (turbo)	V_I = V_{CC} or GND No load, f = 1.0 MHz note (7)		90	140 (180)	mA

CAPACITANCE

Note (4)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1.0 MHz		15	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1.0 MHz		15	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V f = 1.0 MHz		25	pF

AC CHARACTERISTICS Note (5)

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)
(V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial)
(V_{CC} = 5V ± 10%, T_C = -55°C to 125°C for Military)*

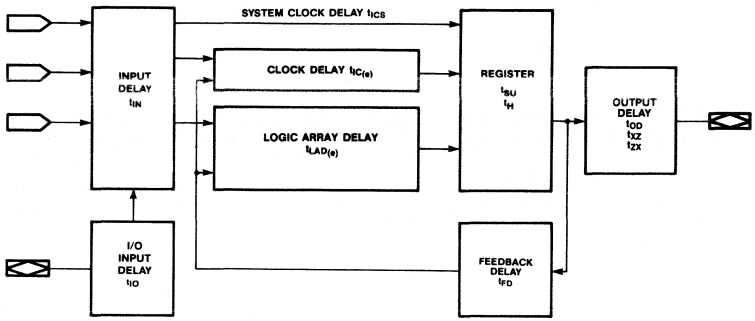
			EP1800-2		EP1800-3		EP1800		NON-TURBO ADDER note (5)		
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNIT**
t_{PD1}	Input to non-registered output	C_1 = 50pF (Fig 8)		65		75		85		30	ns
t_{PD2}	I/O input to non-registered output			70		80		90		30	ns
t_{IN}	Input pad and buffer delay			10		12		14		0	ns
t_{IO}	I/O input pad and buffer delay			5		5		5		0	ns
t_{LADe}	Enhanced Logic Array delay			35		39		43		30	ns
t_{LAD}	Logic Array delay			40		44		48		30	ns
t_{OD}	Output buffer and pad delay	C_1 = 50 pF (Fig 8)		15		19		23		0	ns
t_{ZX}	Output buffer enable			15		19		23		0	ns
t_{XZ}	Output buffer disable	C_1 = 5 pF note (2)		15		19		23		0	ns
f_{max}	Maximum clock frequency	note (10)	20.8		18.5		16.1		0		MHz
t_{SU}	Register set-up time		12		14		18		0		ns
t_{HS}	Register hold time (system clock)		0		0		0		0		ns
t_H	Register hold time		30		30		30		0		ns
t_{CH}	Clock high time		24		27		30		0		ns
t_{CL}	Clock low time		24		27		30		0		ns
t_{ICe}	Enhanced clock delay			35		39		43		30	ns
t_{IC}	Clock delay			40		44		48		30	ns
t_{ICS}	System clock delay			4		4		4		0	ns
t_{FD}	Feedback delay			10		14		16		-30	ns
t_{CLRe}	Enhanced register clear time			35		39		43		30	ns
t_{CLR}	Register clear time			40		44		48		30	ns
t_{CNT}	Minimum clock period (register output feedback to register input - internal data)			62		72		82		0	ns
f_{CNT}	Internal maximum frequency ($1/t_{CNT}$)	note (7)	16.2		13.8		12.2		0		MHz

Notes:
1. Typical values are for T_A = 25°C, V_{CC} = 5V
2. Sample tested only for an output change of 500mV.
3. Minimum DC input is -0.3V. During transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
4. Capacitance measured at 25°C. Sample tested only. Clock pin capacitance for dedicated clock inputs only. Pins 17, 19, 51, 53, (high voltage pin during programming), has capacitance of 160 pF max.
5. See TURBO-BIT, page 2-13.
6. Figures in ( ) pertain to military temperature version.
7. Measured with device programmed as four 12-Bit Counters.
8. EPLD automatically goes into standby mode if logic transitions do not occur when in non-turbo mode (approximately 100 ns after last transition).
9. Clock t_r/t_f = 250ns, (100ns).
10. The f_{MAX} values shown represent the highest frequency for pipelined data.

GRADE	AVAILABILITY	
Commercial (0°C to 70°C)	EP1800-2	EP1800-3 EP1800
Industrial (-40°C to 85°C)		EP1800-3 EP1800
Military (-55°C to 125°C)		EP1800

*** Specifications for MIL-STD-883 devices may vary from those above. A Military Product Drawing, prepared in accordance with appropriate military specification formats, is available to provide guidance for the preparation of Source Control Drawings (SCD). Please contact Altera Marketing at (408) 984-2800 x 101 to obtain 883 Product drawings.**

FIG. 9 MACROCELL DELAY PATHS

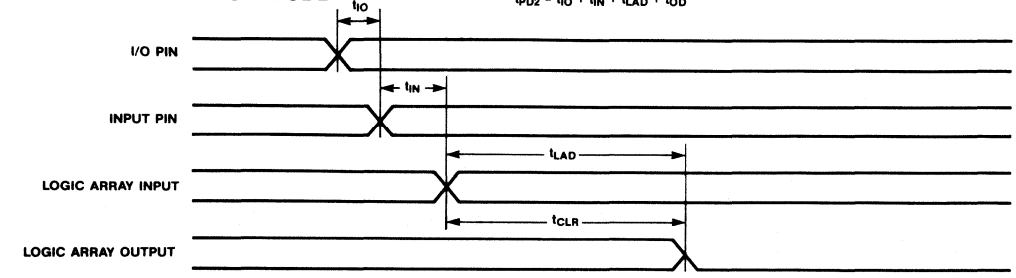


NOTE: If register is by-passed, the delay between logic array and output buffer is zero.

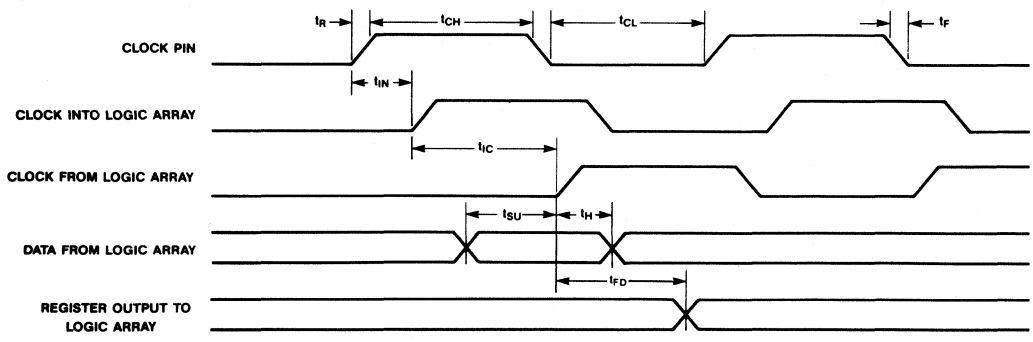
FIG. 10 SWITCHING WAVEFORMS

INPUT MODE

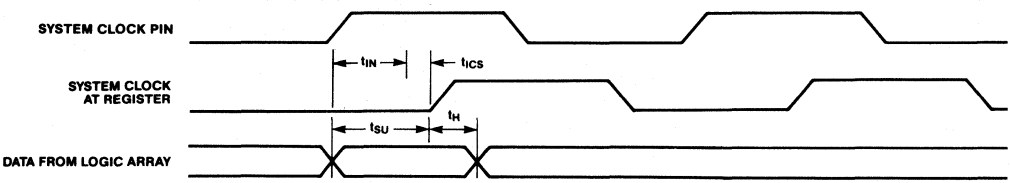
$t_{PD1} = t_{IN} + t_{LAD} + t_{OD}$
$t_{PD2} = t_{IO} + t_{IN} + t_{LAD} + t_{OD}$



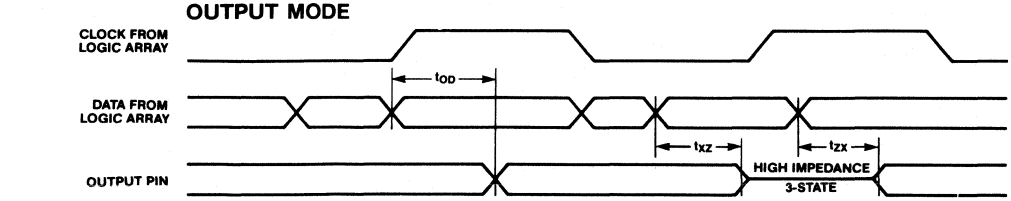
CLOCK MODE



SYSTEM CLOCK MODE



OUTPUT MODE

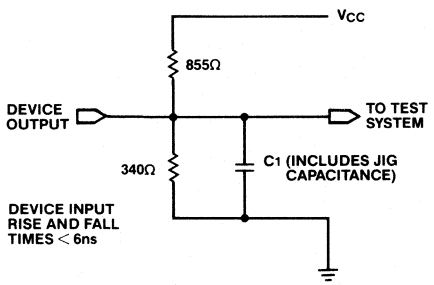


FUNCTIONAL TESTING

The EP1800 is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

The erasable nature of the EP1800 allows test programs to be used and then erased during early stages of the production flow. This facility to use application-independent, general purpose tests is called generic testing and is unique among user-defined LSI logic devices. The devices also contain on board test circuitry to allow verification of function and AC specification once encapsulated in non-window packages.

FIG. 8 AC TEST CONDITIONS



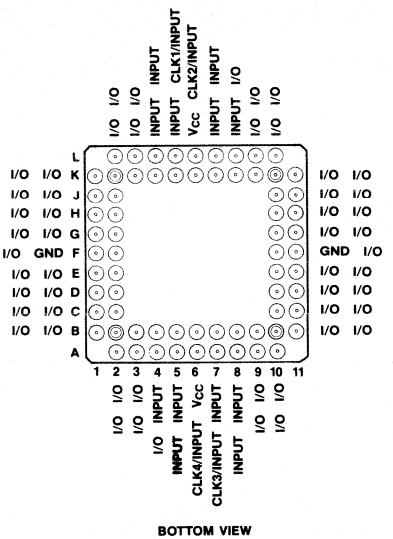
Power supply transients can affect AC measurements, simultaneous transitions of multiple outputs should be avoided for accurate measurement. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

TURBO-BIT

Some EPLDs contain a programmable option to control the automatic power down feature that enables the low standby power mode of the device. This option is controlled by a TURBO-BIT which can be set using A+PLUS. When the TURBO-BIT is programmed (Turbo = ON), the low standby power mode (Icc1) is disabled. This renders the circuit less sensitive to Vcc noise transients which can be created by the power-up/power-down cycle when operating in the low power mode. The typical Icc vs frequency data for both Turbo and Non-Turbo (low power) mode is shown in each EPLD data sheet. All AC values are tested with the TURBO-BIT programmed.

If the design requires low power operation then the TURBO-BIT should be disabled (Turbo = OFF). When operating in this mode, some AC parameters are subject to increase. Values given in the AC specifications section under "Non-Turbo Adder" must be added to the respective AC parameter to determine worst-case timing.

PGA CONNECTION DIAGRAM



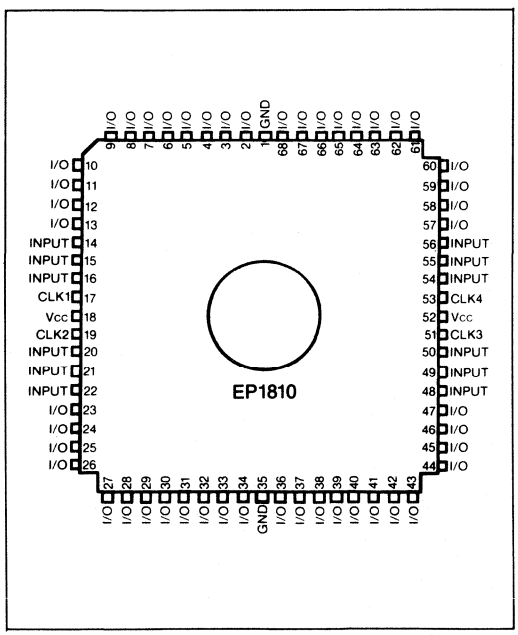
HIGH PERFORMANCE 48-MACROCELL EPLD

EP1810

FEATURES

- High density, user-configurable LSI logic replacement for conventional and custom logic.
- Functional and pin compatible with the Altera EP1800.
- 30 MHz clock rates.
- "Zero Power" (typically 35 μA standby).
- 48 Macrocells with configurable I/O architecture allowing 64 inputs or 48 outputs.
- Programmable registers providing D, T, SR or JK flipflops with individual Asynchronous Clear control.
- Programmable clock option allows independent clocking of all registers.
- TTL/CMOS I/O compatibility.
- 100% generically testable-provides 100% programming yield.
- Programmable "Security Bit" allows total protection of proprietary designs.
- CAD support from Altera's A+PLUS Development System featuring schematic capture design entry with extensive Primitive and TTL libraries.
- Package in a 68 pin (window) and plastic (one time programmable) JLCC, PLCC and PGA configurations.

CONNECTION DIAGRAM



GENERAL DESCRIPTION

The Altera EP1810 is an enhanced performance, pin-compatible version of the popular EP1800 Erasable Programmable Logic Device (EPLD). Available in 68-pin PGA and 68-pin J-leaded chip carrier packages, the EP1810 contains 48 Macrocells with user-configurable I/O architecture, allowing up to 64 inputs and 48 outputs.

Each of the 48 Macrocells contains a programmable AND and fixed OR PLA structure, see EP1800 datasheet, with a maximum eight product terms for logic implementation. In addition, single product terms control Output Enable/Asynchronous Clock and Asynchronous Clear functions.

The Altera proprietary programmable I/O architecture allows the EP1810 user to program output and feedback paths for both combinatorial or registered operation, active high or active low.

For increased flexibility, the EP1810 also includes programmable registers. Each of the 48 internal registers may be programmed to be D, T, SR or JK flipflop. In addition, each register may be clocked asynchronously on an individual basis or synchronously on a banked register basis.

For proper operation, standard high performance design practices should be followed. It is recommended that opaque labels be placed over device window. Input and output pins must be constrained to the range GND $\leq$ (V_{IN} or V_{OUT}) $\leq$ V_{CC}. Unused inputs must always be tied to an appropriate logic level (e.g. either V_{CC} or GND). Each set of V_{CC} and GND pins must be shorted together directly at the device. Power supply decoupling capacitors of at least .2μF must be connected between each V_{CC} pin and GND. For the most effective decoupling, connect one capacitor between each set of V_{CC} and GND pins, directly at the device.

Programming the EP1810 is accomplished by using the Altera A+PLUS PC-based development software which supports schematic capture, netlist, state machine and Boolean equation design entry methods. Once the design is entered, A+PLUS automatically performs translation into logical equations, Boolean minimization, and design fitting directly to an EP1810. The device may then be programmed to achieve customized working silicon within minutes at the designer's own desktop.

For full EP1810 functional description please consult the EP1800 datasheet.

ADVANCED INFORMATION

SPECIFICATIONS SUBJECT TO CHANGE

REV. 1.0

ALTERA

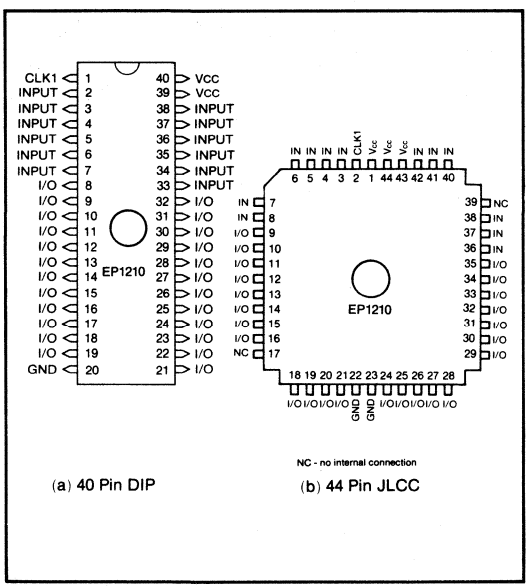
28 MACROCELL EPLD

EP1210

FEATURES

- High Density (over 1200 gates) replacement for TTL and 74HC.
- Advanced CHMOS EPROM technology allows for erasability and reprogrammability.
- Low power: 15 mW typical standby power dissipation.
- Programmable Macrocell & I/O Architecture: up to 36 inputs or 24 outputs, 28 Macrocells including 4 buried state registers.
- Programmable latch feature allows latching of all inputs.
- Programmable clock system for input latches and output registers.
- Product term sharing and local bus architecture for optimized array performance.
- 100% generically testable — provides 100% programming yield.
- Programmable "Security Bit" allows total protection of proprietary designs.
- Advanced software support featuring Schematic Capture, Interactive Netlist, State Machine and Boolean Equation design entry methods.
- Package options include 40 pin DIP and 44 pin J-Leaded Chip Carrier.

CONNECTION DIAGRAM



NC - no internal connection

(a) 40 Pin DIP

(b) 44 Pin JLCC

GENERAL DESCRIPTION

The Altera EP1210 is an LSI logic circuit that can be programmed to provide logic replacement for conventional SSI and MSI logic circuits.

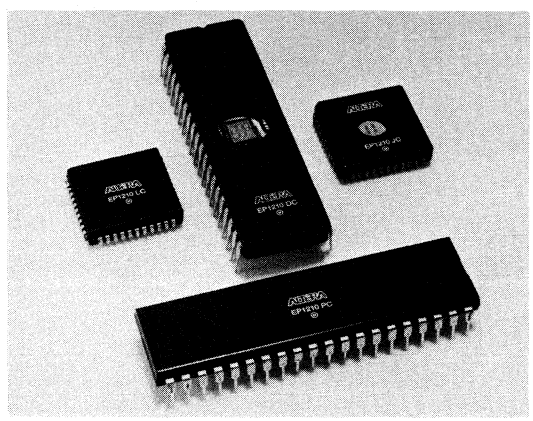
The EP1210 contains CMOS EPROM (floating-gate) elements that control the logical operation of the device. The device can typically provide equivalent performance to 1200 gates of SSI and MSI logic. The EPROM technology enables the logic designer to rapidly program the device and make design changes after erasing for just a few minutes. The same technology also permits 100% factory testing of all elements within the device.

The CMOS technology reduces power consumption to less than 10% of equivalent bipolar devices without sacrificing speed performance.

To implement general purpose logic the EP1210 contains the familiar sum-of-product PLA structure with a programmable AND and fixed OR array. The design uses a range of OR gate widths to accommodate logical functions without the overhead of unnecessary product-terms or the speed penalties of programmable OR structures.

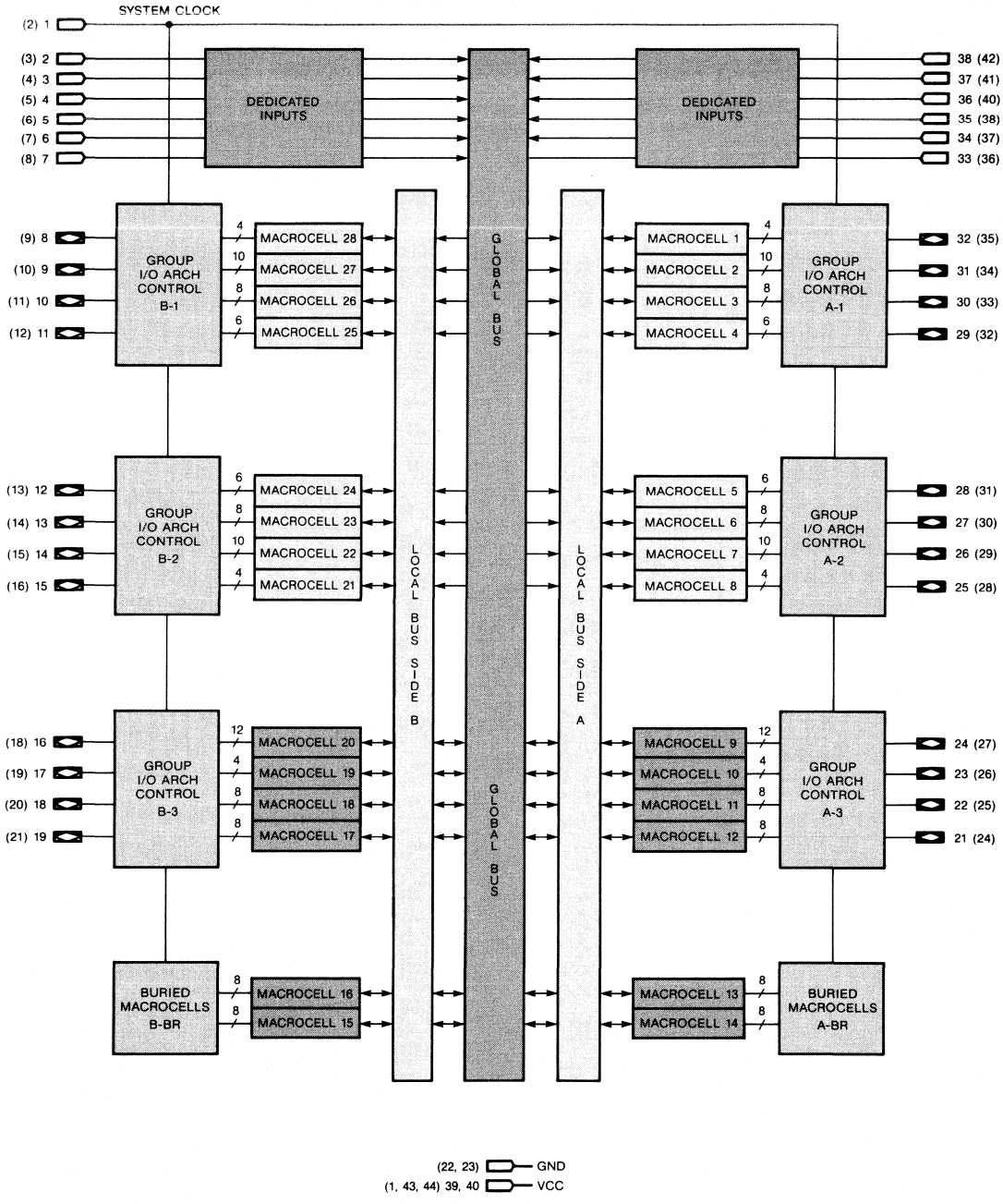
A segmented PLA design that provides local and global connectivity also optimizes the performance of the EP1210.

The EP1210 contains innovative architectural features that provide significant I/O flexibility and maximize performance within a conventional dual-in-line package or a J-leaded chip carrier package for increased footprint efficiency.



REV. 4.0

EP1210 BLOCK DIAGRAM



PIN NUMBERS IN ( ) PERTAIN TO 44 PIN JLCC.

FUNCTIONAL DESCRIPTION

The EP1210 is an LSI erasable programmable logic device (EPLD) which uses EPROM technology to configure connections within a programmable logic array. The device has a programmable I/O architecture that provides options to change inputs, outputs and logical function of the device.

The internal architecture is based on 28 Macrocells each of which contains a PLA and a programmable I/O block that can be programmed to create many different logic structures. This powerful I/O architecture can be configured to support both active-high, active-low, 3-state, open-drain and bi-directional data ports or act as an input, all on a 4-bit wide basis.

All inputs to the circuit may be latched, including the 12 dedicated input pins.

The Macrocells share a common programmable clock system that controls clocking of all registers and input latches. The device contains 8 modes of clock operation that allow logic transitions to take place on either rising or falling edges of the clock signals.

The primary logic array of the EP1210 is segmented into two symmetrical halves that communicate via global bus signals. The main arrays contain some 15104 programmable elements representing 236 product terms each containing 64 input signals.

Macrocells in each half of the circuit are grouped together for architecture programming. These banks of four Macrocells can be further programmed on an individual Macrocell basis to generate active high or active low outputs of the logic function from the PLA.

The circuit further contains four Macrocells whose outputs are only fed back into the array to create buried-state functions. The feedback path may be either the registered or combinatorial result of the PLA output. The use of buried state Macrocells provides maximum equivalent logic density without demanding higher pin-count packages which consume valuable board space.

I/O ARCHITECTURE

The Input/Output architecture of the EP1210 Macrocells can be programmed using both static and dynamic controls. The static controls remain fixed after the device is programmed whereas the dynamic controls may change state as a result of the signals applied to the device.

The static controls set the inversion logic, register by-pass and input feedback multiplexers. In the latter two cases these controls operate on four Macrocells as a bank. The buried-state registers have simpler controls which determine if the feedback is to be registered or combinatorial.

The dynamic controls consist of a programmable input latch-enable, as well as register clear and output-enable product terms. The latch-enable function is common throughout the EP1210 and is programmed by the clock control block but may also be driven by input signals applied to pin 1 (see clock modes in Table 1). The register clear and output-enable controls are logically controlled by single product terms (the logic AND of programmed variables in the array). These terms have control over banks of four Macrocells.

The output-enable control may be used to generate architecture types that include bi-directional, 3-state, open-drain or input only structures.

OUTPUT/FEEDBACK SELECTION

The EP1210 Input/Output Architecture allows each group of Macrocells to be programmed for combinatorial or registered operation, with individual control over output polarity. In addition, the designer may configure the feedback path for combinatorial, registered, input (pin), and latched input feedback. All Macrocell groups have Asynchronous Clear control from a dedicated product term. When the product term is asserted to a logical "1", the registers within the respective Macrocell group will immediately be loaded with a logical "0" independently of the clock. On power up, the EP1210 performs the Clear function automatically.

Figure 2 shows the basic output configurations for the EP1210. In a combinatorial mode, the output is controlled via the group dedicated Output Enable product term. The Invert Select EPROM bit controls output polarity. The Feedback Select Multiplexer enables registered feedback, pin or latched pin feedback, or no feedback.

In a registered mode, 4 to 16 product terms are ORed together and made available to the D-type flipflop. The Output Enable product term allows registered or no output. The Invert Select EPROM bit determines output polarity. The Feedback Select Multiplexer can be configured for registered feedback, pin or latched pin feedback, or no feedback.

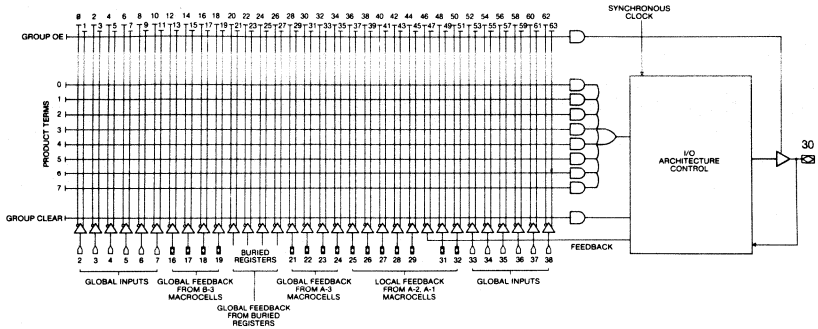
Any I/O group can be configured as a dedicated input group by selecting no output and pin feedback.

In the erased state, the EP1210 I/O is configured for active low combinatorial output and latched pin feedback.

SHARED PRODUCT TERMS

Macrocells 9, 10, 11, 12, 17, 18, 19 and 20 have the facility to share a total of 16 additional product terms. The sharing takes place between pairs of adjacent macrocells. This capability enables, for example, Macrocells 9 and 10 to expand to 16 and 8 effective product terms respectively and for Macrocells 11 and 12 both to expand to 12 effective product terms. This facility is primarily of use in state machine and counter applications where common product-terms are frequently required among output functions.

FIG. 1 LOGIC ARRAY MACROCELL (FOR OUTPUT TAKEN FROM "A" HALF ONLY)

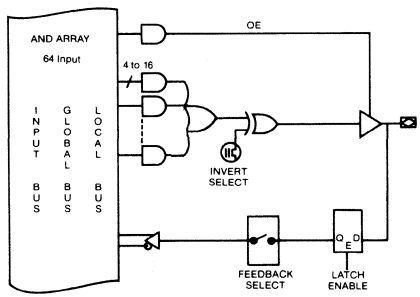


Note: ⊠ = I/O Pin in which Logic Array input is from feedback path pin numbers pertain to 40 pin DIP.

FIG. 2 MACROCELL CONFIGURATIONS

A. I/O MACROCELLS

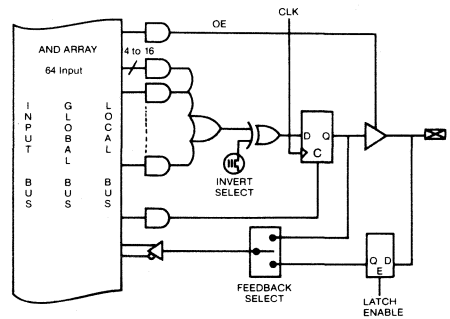
COMBINATORIAL



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
Combinatorial/High	Pin, Latched Pin None
Combinatorial/Low	Pin, Latched Pin None
None	Pin, Latched Pin

REGISTERED

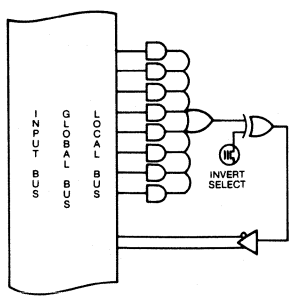


I/O SELECTION

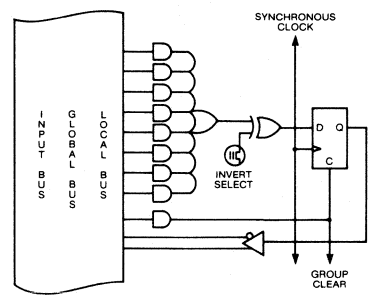
OUTPUT/POLARITY	FEEDBACK
Registered/High	Registered, Pin, Latched Pin, None
Registered/Low	Registered, Pin, Latched Pin, None
None	Registered, Pin, Latched Pin

B. BURIED MACROCELLS

NO OUTPUT, COMBINATORIAL FEEDBACK



NO OUTPUT, REGISTERED FEEDBACK



BUS STRUCTURE

The two identical halves of the EP1210 communicate via a series of buses. The local bus structure that is used for communication within each half of the chip contains 16 conductors that carry the TRUE and COMPLEMENT of 8 local Macrocells.

The global bus is comprised of 48 conductors that span the entire chip which carry the TRUE and COMPLEMENT of primary inputs (pins 2 through 7 and 33 through 38), signals from 4 Buried Registers, as well as the global outputs of 8 Macrocells in groups A-3 and B-3.

MACRO — BUS INTERFACE

The Macrocells within an EP1210 are interconnected to other Macrocells and inputs to the device via three internal data buses.

The product-terms span the entire bus structure that is adjacent to their Macrocell so that they may produce a logical AND of any of the variables (or their complements) that are present on the buses.

Macrocells all have the ability to return data to the local or global bus. Feedback data may originate from the output of the Macrocell or from the I/O pin. Feedback to the global bus communicates throughout the part. Macrocells that feedback to the local bus communicate to only half the EP1210. Connections to and from the signal buses are made with EPROM

FIG. 3 MACROCELL BUS STRUCTURE

At each intersecting point in the logic array there exists an EPROM-type programmable connection. Initially, all connections are complete. This means that both the true and complement of all inputs are connected to each product-term. Connections are opened during the programming process. Therefore any product term can be connected to the true or complement of any input. When both the true and complement connections of any input are left intact, a logical false results on the output of the AND gate. If both the true and complement connections of any input are programmed open, then a logical "don't care" results for that input. If all inputs for a product term are programmed open, then a logical true results on the output of the AND gate.

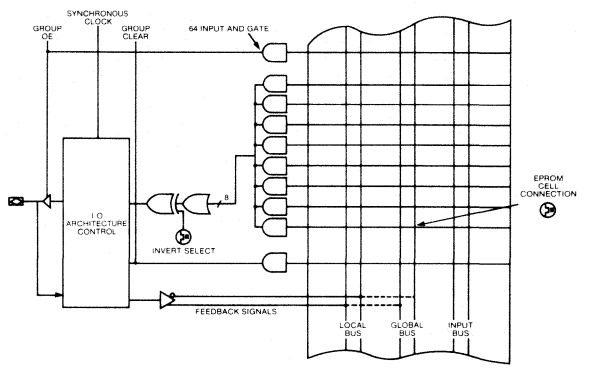
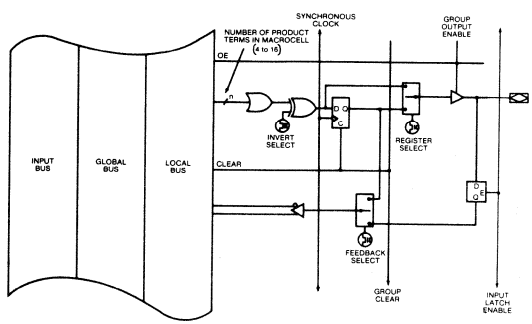
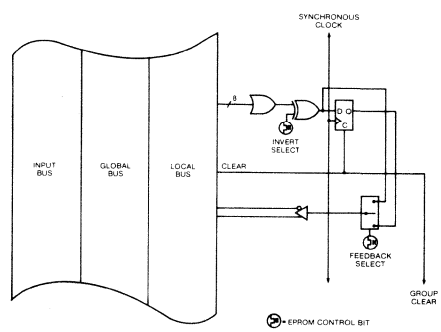


FIG. 4

A. I/O MACROCELL



B. BURIED MACROCELL



switches that provide the reprogrammable logic capability of the circuit.

Macrocells in groups A-3 and B-3 and the buried registers all have global bus connections while Macrocells in groups A-1, A-2, and B-1, B-2 have local bus connections. Figure 3 illustrates the local and global bus connections. Advanced features of the ALTERA development system will, if desired, automatically select an appropriate Macrocell to meet both the logic requirements and the connection to an appropriate signal bus to achieve the interconnection to other Macrocells.

CLOCK MODE CONTROL

The EP1210 contains two internal clock data paths that drive the input latches (transparent 7475 type) and the output registers. These clocks may be programmed into one of eight operating modes. Input latches may be enabled on either the high or low level of CLK1 (pin1). Once latched, the input signal keeps its value until the next transition of the chosen clock. Output registers can be programmed to be positive or negative edge-triggered with respect to CLK1 or CLK2. Table 1 shows the operation of each programming mode.

In the erased state, the EP1210 clocking operation is set for mode 0. This means inputs are latched on a high level of CLK1. The high to low transition of CLK1 causes the input latches to become disabled, allowing input values to propagate into the logic array without being latched. In addition, CLK1 drives the output registers which are negative edge-triggered.

Care is required when using any of the two-clock modes to ensure that timing hazards are not created.

TABLE 1 CLOCK PROGRAMMING

PROGRAMMED MODE	INPUT SIGNALS ARE PASSED (a) AND DATA IS LATCHED (b) WHEN:	OUTPUT REGISTERS CHANGE STATE WHEN:	CLOCK CONFIGURATION
0	CLK1 (PIN1) a b	CLK1 (PIN1)	1 CLOCK
1	CLK1 (PIN1) a b	CLK1 (PIN1)	1 CLOCK
2	INPUTS NOT LATCHED	CLK1 (PIN1)	1 CLOCK
3	INPUTS NOT LATCHED	CLK1 (PIN1)	1 CLOCK
4	CLK1 (PIN1) a b	CLK2 (PIN38)	2 CLOCKS
5	CLK1 (PIN1) a b	CLK2 (PIN38)	2 CLOCKS
6	CLK1 (PIN1) a b	CLK2 (PIN38)	2 CLOCKS
7	CLK1 (PIN1) a b	CLK2 (PIN38)	2 CLOCKS

FIG. 5 PROGRAMMABLE CLOCK CONTROL SYSTEM

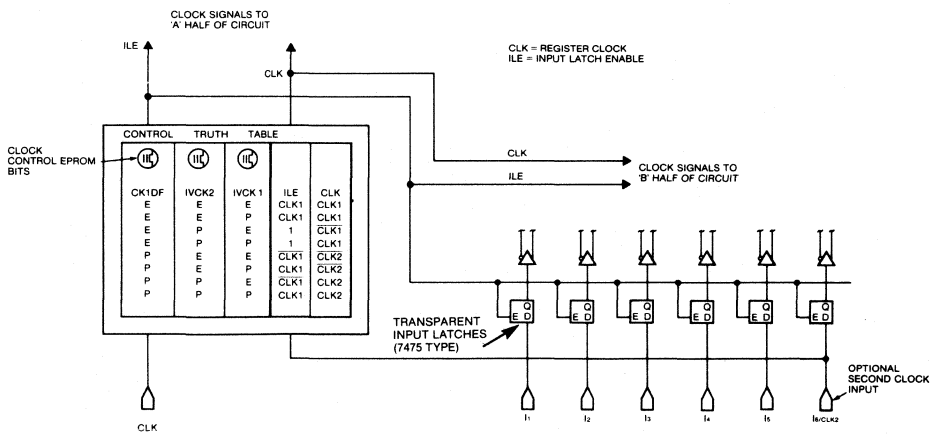
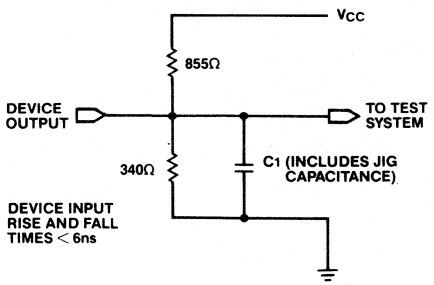


FIG. 7 AC TEST CONDITIONS



Power supply transients can affect AC measurements, simultaneous transitions of multiple outputs should be avoided for accurate measurement. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

FIG. 8 ICC VS. FMAX

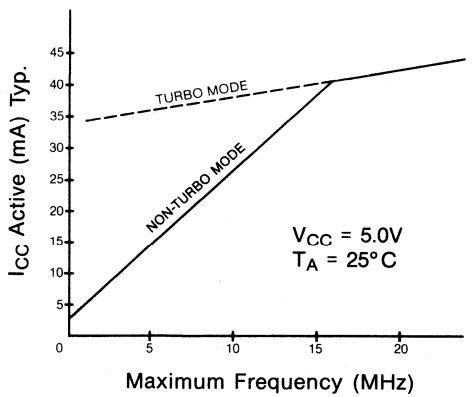
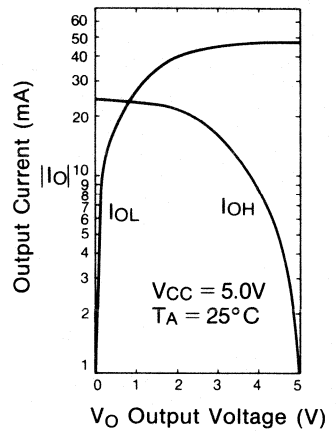


FIG. 9 OUTPUT DRIVE CURRENTS



TURBO-BIT

Some EPLDs contain a programmable option to control the automatic power down feature that enables the low standby power mode of the device. This option is controlled by a TURBO-BIT which can be set using A+PLUS. When the TURBO-BIT is programmed (Turbo = ON), the low standby power mode (Icc1) is disabled. This renders the circuit less sensitive to Vcc noise transients which can be created by the power-up/power-down cycle when operating in the low power mode. The typical Icc vs frequency data for both Turbo and Non-Turbo (low power) mode is shown in each EPLD data sheet. All AC values are tested with the TURBO-BIT programmed.

If the design requires low power operation then the TURBO-BIT should be disabled (Turbo = OFF). When operating in this mode, some AC parameters are subject to increase. Values given in the AC specifications section under "Non-Turbo Adder" must be added to the respective AC parameter to determine worst-case timing.

FUNCTIONAL TESTING

The EP1210 is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

As a result, traditional problems associated with fuse-programmed circuits are eliminated. The erasable nature of the EP1210 allows test program patterns to be used and then erased. This facility to use application-independent, general purpose tests is called generic testing and is unique among user-defined LSI logic devices.

DESIGN SECURITY

The EP1210 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

ABSOLUTE MAXIMUM RATINGS

Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	With respect to GND note (3)	-2.0	7.0	V
V_{PP}	Programming supply voltage		-2.0	13.5	V
V_I	DC INPUT voltage		-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		-150	+150	mA
I_{OUT}	DC OUTPUT current, per pin		-25	+25	mA
P_D	Power dissipation			650	mW
T_{STG}	Storage temperature	No bias	-65	+150	°C
T_{AMB}	Ambient temperature	Under bias	-65	+135	°C
ESD	ElectroStatic Discharge Voltage		±900		V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage	note (6)	4.75 (4.5)	5.25 (5.5)	V
V_I	INPUT voltage		0	V_{CC}	V
V_O	OUTPUT voltage		0	V_{CC}	V
T_A	Operating temperature	For Commercial	0	70	°C
T_A	Operating temperature	For Industrial	-40	85	°C
T_C	Case temperature	For Military	-55	125	°C
T_R	INPUT rise time			500	ns
T_F	INPUT fall time			500	ns

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)
(V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial)
(V_{CC} = 5V ± 10%, T_C = -55°C to 125°C for Military)*
Note (1) and (6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3		0.8	V
V_{OH}	HIGH level TTL output voltage	I_{OH} = -4mA DC	2.4			V
V_{OH}	HIGH level CMOS output voltage	I_{OH} = -2mA DC	3.84			V
V_{OL}	LOW level output voltage	I_{OL} = 4mA DC			0.45	V
I_I	Input leakage current	V_O = V_{CC} or GND	-10		+10	µA
I_{OZ}	3-state output off-state current	V_I = V_{CC} or GND	-10		+10	µA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND No load note (8)		3	6 (9)	mA
I_{CC2}	V_{CC} supply current (non-turbo)	V_I = V_{CC} or GND No load, f = 1.0 MHz note (7)		6	10 (13)	mA
I_{CC3}	V_{CC} supply current (turbo)	V_I = V_{CC} or GND No load, f = 1.0 MHz note (7)		35	65 (75)	mA

CAPACITANCE

Note (4)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1.0 MHz		30	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1.0 MHz		40	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V f = 1.0 MHz		30	pF

AC CHARACTERISTICS Note (5)

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)
(V_{CC} = 5V ± 10%, T_A = –40°C to 85°C for Industrial)
(V_{CC} = 5V ± 10%, T_C = –55°C to 125°C for Military)*

			EP1210-1		EP1210-2		EP1210		NON-TURBO ADDER note (5)		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t_{PD1}	Input to non-registered output	C_1 = 30pF		55		65		90		10	ns
t_{PD2}	I/O input to non-registered output			58		68		93		10	ns
t_{PZX}	Input to output enable			55		65		90		10	ns
t_{PXZ}	Input to output disable	C_1 = 5pF note (2)		55		65		90		10	ns
t_{CLR}	Asynchronous output clear time	C_1 = 30pF		90		110		150		10	ns
t_{IO}	I/O input buffer delay			3		3		3		0	ns

SYNCHRONOUS CLOCK MODE

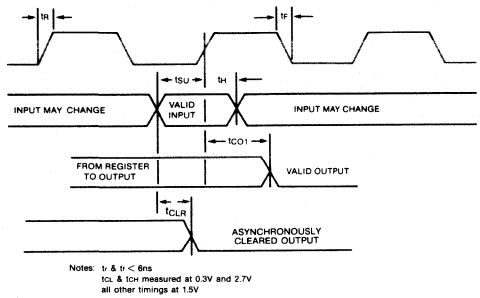
			EP1210-1		EP1210-2		EP1210		NON-TURBO ADDER		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
f_{MAX}	Maximum frequency	note (9)	26.2		23.2		17.5		0		MHz
t_{SU}	Input setup time		38		43		57		10		ns
t_H	Input hold time		0		0		0		0		ns
t_{CH}	Clock high time		19		21		28		0		ns
t_{CL}	Clock low time		19		21		28		0		ns
t_{CO1}	Clock to output delay			35		40		53		0	ns
t_{CNT}	Minimum clock period (register output feedback to register input - internal path)	note (7)		50		58		80		0	ns
f_{CNT}	Internal maximum frequency ($1/t_{CNT}$)	note (7)	20.0		17.2		12.5		0		MHz
t_{ILS}	Set up time for latching inputs		0		0		0		0		ns
t_{ILH}	Hold time for latching inputs		17		20		25		0		ns
t_{C1C2}	Minimum clock 1 to Clock 2 delay			44		50		65		0	ns
t_{P3}	Minimum period for a 2-clock system ($t_{C1C2} + t_{CO1}$)			79		90		118		0	ns
f_3	Maximum frequency ($1/t_{P3}$)		12.6		11		8.5		0		MHz

Notes:
1. Typical values are for T_A = 25°C, V_{CC} = 5V
2. Sample tested only for an output change of 500mV.
3. Minimum DC input is –0.3V. During transitions, the inputs may undershoot to –2.0V for periods less than 20ns.
4. Capacitance measured at 25°C. Sample tested only.
5. See TURBO-BIT, page 2-21.
6. Figures in ( ) pertain to military temperature version.
7. Measured with device programmed as a 26-Bit Counter.
8. EPLD automatically goes into standby mode if logic transitions do not occur when in non-turbo mode (approximately 100 ns after last transition).
9. The f_{MAX} values shown represent the highest frequency for pipelined data.

GRADE	AVAILABILITY
Commercial (0°C to 70°C)	EP1210-1, EP1210-2, EP1210
Industrial (–40°C to 85°C)	EP1210
Military (–55°C to 125°C)	EP1210

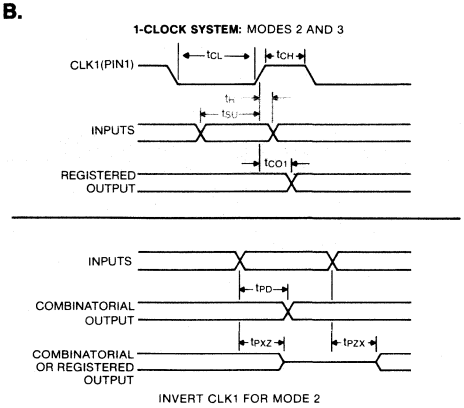
*** Specifications for MIL-STD-883 device may vary from those above. A Military Product Drawing, prepared in accordance with appropriate military specification formats, is available to provide guidance for the preparation of Source Control Drawings (SCD). Please contact Altera Marketing at (408) 984-2800 x 101 to obtain 883 Product drawings.**

FIG. 6 SWITCHING WAVEFORMS A.



Notes: t_R & t_F < 6ns
t_{CL} & t_{CH} measured at 0.3V and 2.7V
all other timings at 1.5V

FIG. 6 SWITCHING WAVEFORMS B.



INVERT CLK1 FOR MODE 2

FIG. 6 SWITCHING WAVEFORMS C.

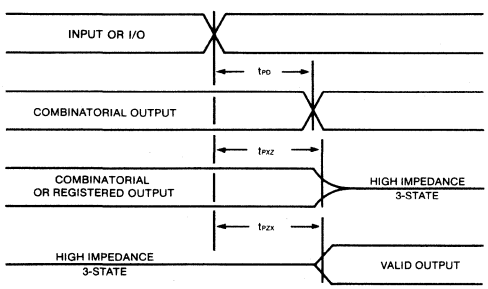
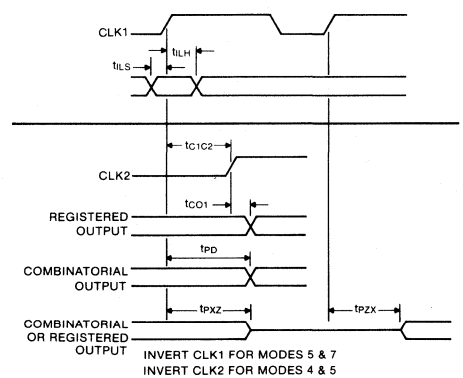
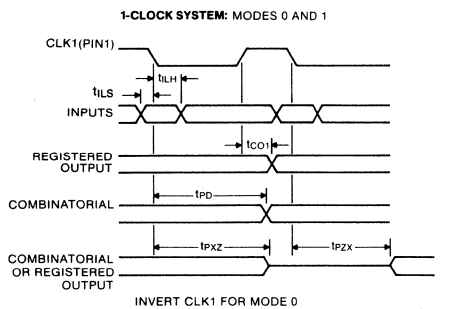


FIG. 6 SWITCHING WAVEFORMS D.



INVERT CLK1 FOR MODES 5 & 7
INVERT CLK2 FOR MODES 4 & 5

FIG. 6 SWITCHING WAVEFORMS E.



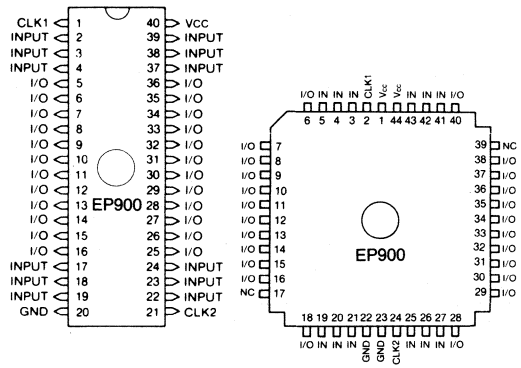
INVERT CLK1 FOR MODE 0

24 MACROCELL EPLD — EP900

FEATURES

- High density (over 900 gates) replacement for TTL and 74HC.
- Advanced CHMOS EPROM technology allows erasability and reprogrammability.
- High speed, t_{pd} = 45ns.
- "Zero Power" (typically 10μA standby)
- Asynchronous clocking of all registers or banked register operation from 2 synchronous clocks.
- 24 Macrocells with configurable I/O architecture allowing 36 inputs and 24 outputs.
- Programmable registers providing D, T, SR or JK flipflops with individual Asynchronous Clear control.
- 100% generically testable—provides 100% programming yield.
- Programmable "Security Bit" allows total protection of proprietary designs.
- Advanced software support featuring Schematic Capture, Interactive Netlist, Boolean Equation and State Machine design entry methods.
- Package options include both a 40 pin, 600 mil DIP and a 44 pin J-leaded chip carrier.

CONNECTION DIAGRAM



(a) 40 Pin DIP

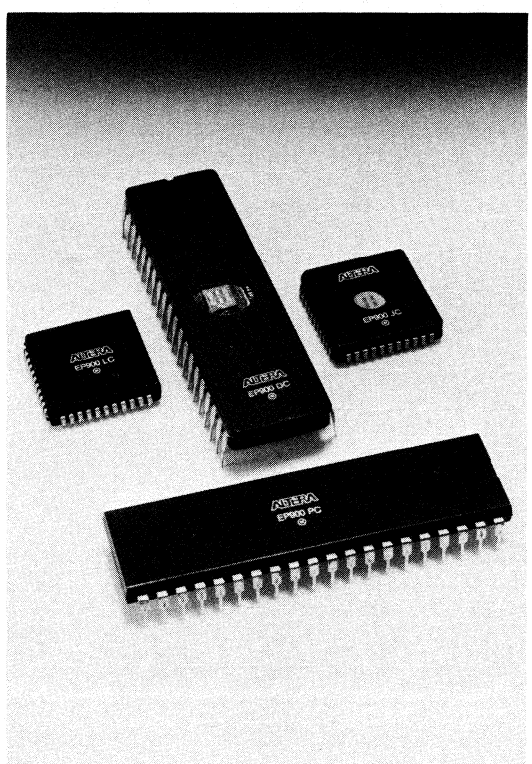
(b) 44 Pin JLCC

GENERAL DESCRIPTION

The ALTERA EP900 Erasable Programmable Logic Device may be used to implement over 900 equivalent gates of SSI and MSI logic, accommodating up to 36 inputs and 24 outputs all within a 40 pin DIP or 44 pin J-leaded chip carrier.

Each of the 24 Macrocells contains a programmable AND, fixed OR PLA structure which yields 8 product terms for logic implementation, and single product terms for Output Enable and Asynchronous Clear control functions.

The ALTERA proprietary programmable I/O architecture allows the EP900 user to program output and feedback paths for both combinatorial or registered operation, active high or active low.



REV. 3.0

For increased flexibility, the EP900 also includes programmable registers. Each of the 24 internal registers may be programmed to be a D, T, SR or JK flipflop. In addition, each register may be clocked asynchronously on an individual basis or synchronously on a banked register basis.

In addition to density and flexibility, the performance characteristics allow the EP900 to be used in the widest possible range of applications. The CHMOS EPROM technology reduces active power consumption to less than 20% of equivalent bipolar devices without a sacrifice in speed performance. This technology also facilitates 100% generic testability as well as UV erasability. As a result, designs and design modifications may be quickly implemented upon a given EP900 without the need for post programming testing.

Programming the EP900 is accomplished by using the ALTERA A+PLUS development software which supports schematic capture, netlist, state machine and Boolean equation design entry methods. Once the design is entered, A+PLUS automatically performs translation into logical equations, Boolean minimization, and design fitting directly to an EP900. The device may then be programmed to achieve customized working silicon within minutes at the designer's own desktop.

FUNCTIONAL DESCRIPTION

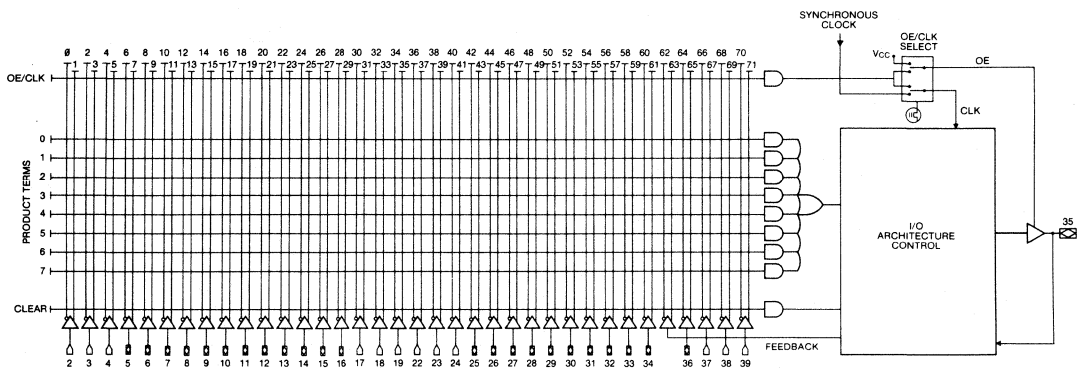
The EP900 is an Erasable Programmable Logic Device (EPLD) in which CMOS EPROM technology is utilized in order to configure connections in a programmable AND logic array. EPROM connections are also used to construct a revolutionary programmable I/O architecture which provides advanced functional capability for user programmable logic.

Externally, the EP900 provides 12 dedicated data inputs, 2 synchronous clock inputs and 24 I/O pins which may be configured for input, output or bi-directional operation.

Figure 1 shows the basic EP900 Macrocell while figure 2 shows the complete EP900 block diagram. The internal architecture is organized with the familiar sum of products (AND-OR) structure. Inputs to the programmable AND array (running vertically in Figure 1) come from the true and complement forms of: 1) the 12 dedicated data inputs and; 2) the 24 feedback signals originating from each of the 24 I/O architecture control blocks. The 72 input AND array encompasses 240 product terms, distributed equally among the EP900's 24 Macrocells. Each product term (running horizontally in Figure 1) represents a 72 input AND gate.

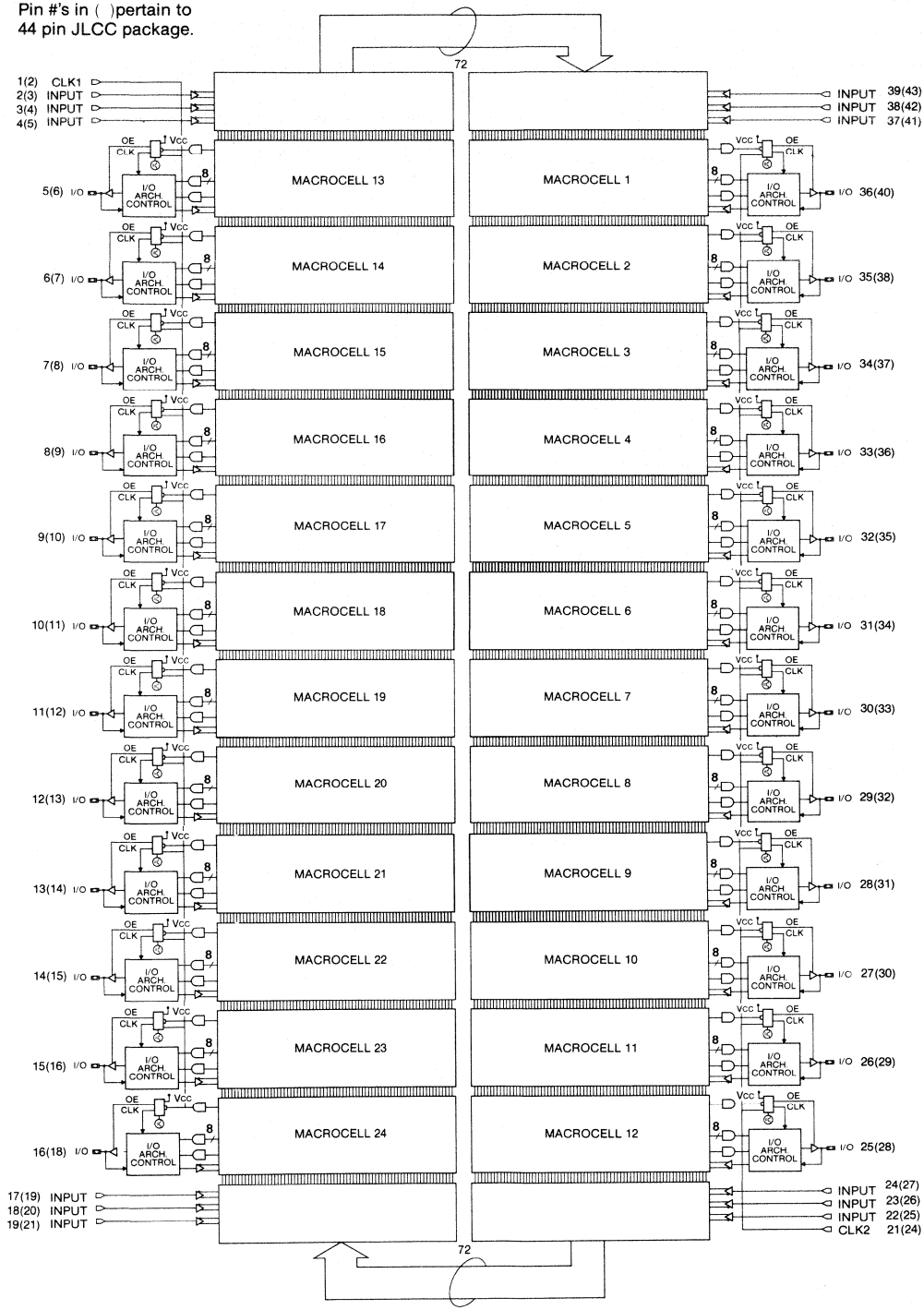
At the intersection point between an AND array input and a product term is an EPROM control cell. In the erased state, all cell connections are made. This means both the true and complement of all array inputs are connected to each product term. During the programming process, selected connections are opened. Therefore, any product term may be connected to the true or complement of any array input signal. When both the true and complement of an array input signal are left connected, a logical false results on the output of the AND gate. If both the true and complement of any array input signal are programmed open, then a logical "don't care" results for that input. If all 72 inputs for a given product term are programmed open, then a logical true results on the output of the corresponding AND gate. Two dedicated clock inputs (these two clock signals are not available in the AND array) provide the clock signals used for synchronous clocking of the EP900 internal registers. Each of these two clock signals is positive edge triggered and has control over a bank of 12 registers. "CLK1" controls Macrocells 13-24, while "CLK2" controls Macrocells 1-12. The EP900 advanced I/O architecture allows any number of the 24 internal registers to be user-defined for synchronous or asynchronous clock modes.

FIG. 1 LOGIC ARRAY MACROCELL



*Note ⊠ = I/O Pin, in which Logic Array input is from feedback path. Pin numbers reflect 40 pin DIP.

FIG. 2 EP900 BLOCK DIAGRAM



I/O ARCHITECTURE

The EP900 Input/Output Architecture provides each Macrocell with over 50 programmable I/O configurations. Each I/O can be configured for combinatorial or registered output, with programmable output polarity. Four different register types (D, T, JK, SR) may be implemented into every I/O without additional logic requirements. I/O feedback selection can also be programmed for registered or input (from the pin) feedback. Another characteristic of the EP900 I/O architecture is the ability to individually clock each internal register from asynchronous clock signals.

OE/CLK Selection

Figure 3 shows the two modes of operation which are provided by the OE/CLK Select Multiplexer. The operation of this multiplexer is controlled by a single EPROM control bit and may be individually configured at each of the 24 I/O pins. In Mode 0, the three-state output buffer is controlled by the OE/CLK product term. (Recall that a single product term is equivalent to a 72 input AND gate.) If the output of the AND gate is a logical true, then the output buffer is enabled. If a logical false resides on the output of the AND gate, then the output buffer is seen as a high impedance node. In this mode the Macrocell flipflop is clocked by its respective synchronous clock input signal (CLK1 or CLK2). After erasure, the OE/CLK Select Mux is configured as Mode 0.

In Mode 1, the Output Enable buffer is tied to VCC (output is always enabled). The Macrocell flipflop may now be triggered from an asynchronous clock signal generated by the OE/CLK product term. This mode allows for individual clocking of flipflops from any of the 72 available AND array input signals. With both true and complement signals in the AND array, the flipflop may be configured to trigger on a rising or falling edge. In addition, this product term controlled clock configuration allows for the implementation of gated clock structures.

Figure 4 shows the basic output configurations available in the EP900. Along with combinatorial output, four register types are available. Each Macrocell may be individually configured. All registers have an individual Asynchronous Clear function which is controlled by a dedicated product term. When this product term yields a logical "1," the Macrocell register will immediately be loaded with a logical "0" independently of the clock. Upon power up of the EP900, the Clear function is performed automatically.

In the Combinatorial configuration, eight product terms are ORed together to acquire the output signal. The Invert Select EPROM bit controls output polarity and the Output Enable buffer is product term controlled. The Feedback Select Multiplexer allows the user to choose I/O (pin) feedback or no feedback to the AND array.

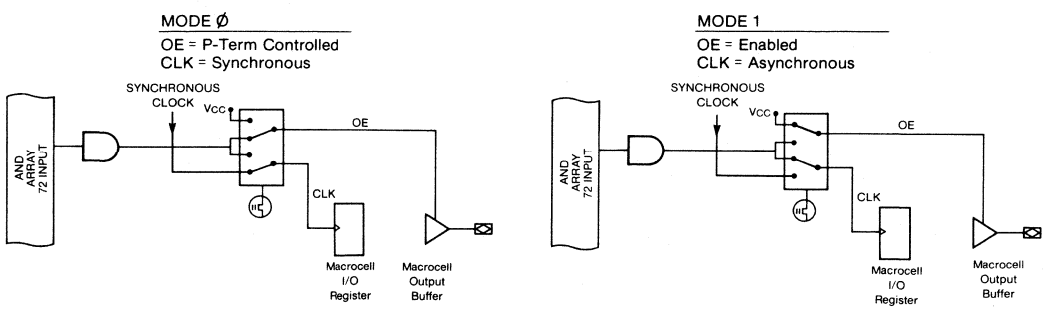
When the D or T register is selected, eight product terms are ORed together and made available to the register input. The Invert Select EPROM bit controls output polarity. The OE/CLK Select Multiplexer is used to configure the mode of operation (Mode 0 or Mode 1... see Figure 3). The Feedback Select Multiplexer allows the user to choose registered, I/O (pin) or no feedback to the AND array.

If the JK or SR register is selected, eight product terms are shared between two OR gates whose outputs feed the two primary register inputs. The allocation of product terms for each register input is optimized by the A+PLUS development software. The Invert Select EPROM bits control output polarity while the OE/CLK Select Multiplexer allows the mode of operation to be Mode 0 or Mode 1. The Feedback Select Multiplexer allows the user to choose registered or no feedback to the AND array.

Any I/O pin may be configured as a dedicated input by selecting no output with I/O (pin) feedback.

In the erased state, the I/O architecture is configured for combinatorial active low output with I/O (pin) feedback.

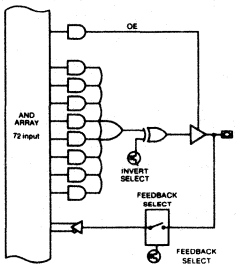
FIG. 3 OE/CLK SELECT MUX



The register is clocked by the synchronous clock signal which is common to 11 other Macrocells. The output is enabled by the logic from the product term.

The output is permanently enabled and the register is clocked via the product term. This allows for gated clocks that may be generated from elsewhere in the EP900.

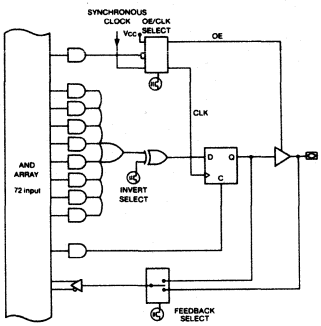
FIG. 4 I/O CONFIGURATIONS



COMBINATORIAL

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
Combinatorial/High	Pin, None
Combinatorial/Low	Pin, None
None	Pin



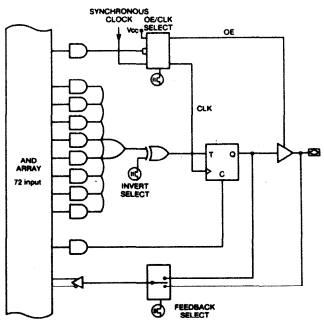
D-TYPE FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
D-Register/High	D-Register, Pin, None
D-Register/Low	D-Register, Pin, None
None	D-Registered
None	Pin

FUNCTION TABLE

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1



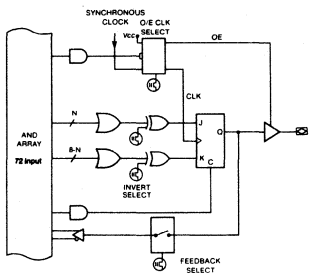
TOGGLE FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
T-Register / High	T-Register, Pin, None
T-Register / Low	T-Register, Pin, None
None	T-Register
None	Pin

FUNCTION TABLE

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0



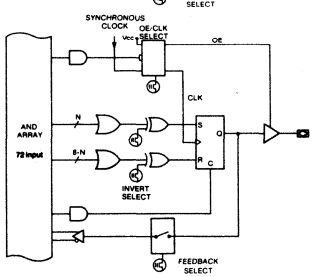
JK FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
JK Register/High	JK Register, None
JK Register/Low	JK Register, None
None	JK Register

FUNCTION TABLE

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



SR FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
SR Register/High	SR Register, None
SR Register/Low	SR Register, None
None	SR Register

FUNCTION TABLE

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1

ABSOLUTE MAXIMUM RATINGS

Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	With respect to GND note (3)	-2.0	7.0	V
V_{PP}	Programming supply voltage		-2.0	13.5	V
V_I	DC INPUT voltage		-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		-150	+150	mA
I_{OUT}	DC OUTPUT current, per pin		-25	+25	mA
P_D	Power dissipation			750	mW
T_{STG}	Storage temperature	No bias	-65	+150	°C
T_{AMB}	Ambient temperature	Under bias	-65	+135	°C
ESD	ElectroStatic Discharge Voltage		±2100		V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage	note (6)	4.75 (4.5)	5.25 (5.5)	V
V_I	INPUT voltage		0	V_{CC}	V
V_O	OUTPUT voltage		0	V_{CC}	V
T_A	Operating temperature	For Commercial	0	70	°C
T_A	Operating temperature	For Industrial	-40	85	°C
T_C	Case temperature	For Military	-55	125	°C
T_R	INPUT rise time	note (9)		500	ns
T_F	INPUT fall time	note (9)		500	ns

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = 0°C to 70°C for Commercial)
(V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial)
(V_{CC} = 5V ±10%, T_C = -55°C to 125°C for Military)*
Note (1) and (6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3		0.8	V
V_{OH}	HIGH level TTL output voltage	I_{OH} = -4mA DC	2.4			V
V_{OH}	HIGH level CMOS output voltage	I_{OH} = -2mA DC	3.84			V
V_{OL}	LOW level output voltage	I_{OL} = 4mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	-10		+10	µA
I_{OZ}	3-state output off-state current	V_O = V_{CC} or GND	-10		+10	µA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND No load note (8)		35	150	µA
I_{CC2}	V_{CC} supply current (non-turbo)	V_I = V_{CC} or GND No load, f = 1.0 MHz note (7)		5	15 (25)	mA
I_{CC3}	V_{CC} supply current (turbo)	V_I = V_{CC} or GND No load, f = 1.0 MHz note (7)		45	75 (100)	mA

CAPACITANCE

Note (4)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1.0 MHz		20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1.0 MHz		20	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V f = 1.0 MHz		20	pF

AC CHARACTERISTICS Note (5)

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)
(V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial)
(V_{CC} = 5V ± 10%, T_C = -55°C to 125°C for Military)*

			EP900-2		EP900-3		EP900		NON-TURBO ADDER note (5)		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t_{PD1}	Input to non-registered output	C_1 = 50pF		45		50		55		25	ns
t_{PD2}	I/O input to non-registered output			50		55		60		25	ns
t_{PZX}	Input or I/O input to output enable			50		55		60		25	ns
t_{PXZ}	Input or I/O input to output disable	C_1 = 5pF note (2)		50		55		60		25	ns
t_{CLR}	Asynchronous output clear time	C_1 = 50pF		50		55		60		25	ns
t_{IO}	I/O input buffer delay			5		5		5		0	ns

SYNCHRONOUS CLOCK MODE

			EP900-2		EP900-3		EP900		NON-TURBO ADDER		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
f_{MAX}	Maximum frequency		26.3		23.8		21.7		0		MHz
t_{SU}	Input or I/O input setup time		38		42		46		25		ns
t_H	Input or I/O input hold time		0		0		0		0		ns
t_{CH}	Clock high time		17.5		20		23		0		ns
t_{CL}	Clock low time		17.5		20		23		0		ns
t_{CO1}	Clock to output delay			23		25		28		0	ns
t_{CNT}	Minimum clock period (register output feedback to register input - internal path)	note (7)		50		55		60		0	ns
f_{CNT}	Internal maximum frequency ($1/t_{CNT}$)	note (7)	20.0		18.2		16.7		0		MHz

ASYNCHRONOUS CLOCK MODE

			EP900-2		EP900-3		EP900		NON-TURBO ADDER		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
f_{MAX}	Maximum frequency		26.3		23.8		21.7		0		MHz
t_{ASU}	Input or I/O input setup time		13		14		15		25		ns
t_{AH}	Input or I/O input hold time		15		15		15		0		ns
t_{ACH}	Clock high time		17.5		20		23		0		ns
t_{ACL}	Clock low time		17.5		20		23		0		ns
t_{ACO1}	Clock to output delay			48		53		59		25	ns
t_{ACNT}	Minimum clock period (register output feedback to register input - internal path)			50		55		60		0	ns
f_{ACNT}	Internal maximum frequency ($1/t_{ACNT}$)		20.0		18.2		16.7		0		MHz

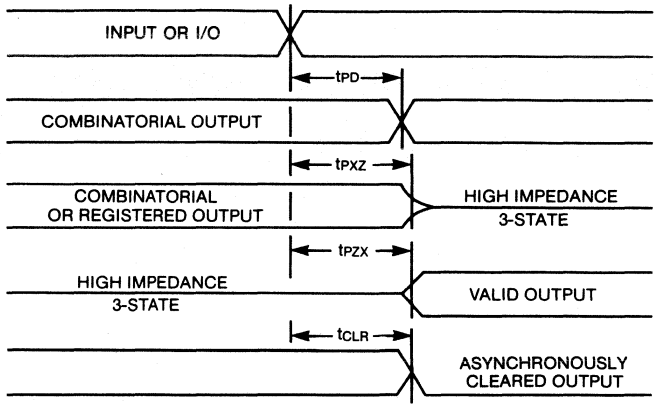
Notes:
1. Typical values are for T_A = 25°C, V_{CC} = 5V
2. Sample tested only for an output change of 500mV.
3. Minimum DC input is -0.3V. During transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
4. Capacitance measured at 25°C. Sample tested only. Clock pin capacitance for dedicated clock inputs only. Pin 21, (high voltage pin during programming), has capacitance of 80 pF max.
5. See TURBO-BIT™, page 2-33.
6. Figures in ( ) pertain to military temperature version.
7. Measured with device programmed as a 24 bit counter.
8. EPLD automatically goes into standby mode if logic transitions do not occur when in non-turbo mode (approximately 100 ns after last transition).
9. Clock t_R, t_F = 250ns (100ns).
10. The f_{MAX} values shown represent the highest frequency for pipelined data.

GRADE	AVAILABILITY
Commercial (0°C to 70°C)	EP900-2 EP900-3 EP900
Industrial (-40°C to 85°C)	EP900
Military (-55°C to 125°C)	EP900

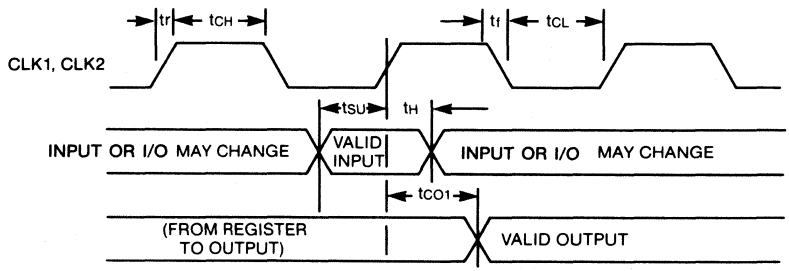
*** Specifications for MIL-STD-883 device may vary from those above. A Military Product Drawing, prepared in accordance with appropriate military specification formats, is available to provide guidance for the preparation of Source Control Drawings (SCD). Please contact Altera Marketing at (408) 984-2800 x 101 to obtain 883 Product drawings.**

FIG. 5 SWITCHING WAVEFORMS

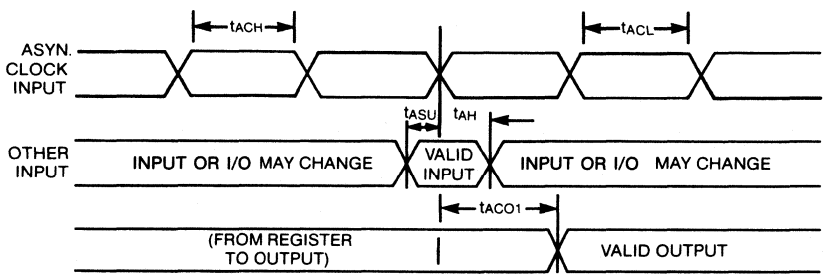
COMBINATORIAL MODE



SYNCHRONOUS CLOCK MODE



ASYNCHRONOUS CLOCK MODE

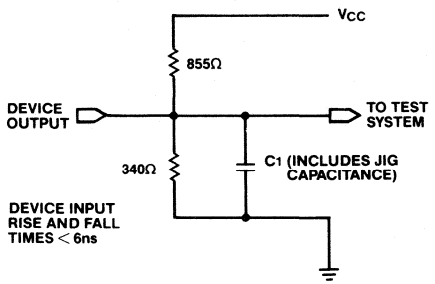


FUNCTIONAL TESTING

The EP900 is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

As a result, traditional problems associated with fuse-programmed circuits are eliminated. The erasable nature of the EP900 allows test programming patterns to be used and then erased. This facility to use application-independent, general purpose tests is called generic testing and is unique among user-defined LSI logic devices.

FIG. 6 AC TEST CONDITIONS



Power supply transients can affect AC measurements, simultaneous transitions of multiple outputs should be avoided for accurate measurement. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

DESIGN SECURITY

The EP900 contains a programmable design security feature that controls access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied nor retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

TURBO-BIT

Some EPLDs contain a programmable option to control the automatic power down feature that enables the low standby power mode of the device. This option is controlled by a TURBO-BIT which can be set using A+PLUS. When the TURBO-BIT is programmed (Turbo = ON), the low standby power mode (Icc1) is disabled. This renders the circuit less sensitive to Vcc noise transients which can be created by the power-up/power-down cycle when operating occurs in the low power mode. The typical Icc vs frequency data for both Turbo and Non-Turbo (low power) mode is shown in each EPLD data sheet. All AC values are tested with the TURBO-BIT programmed.

If the design requires low power operation then the TURBO-BIT should be disabled (Turbo = OFF). When operating in this mode, some AC parameters are subject to increase. Values given in the AC specifications section under "Non-Turbo Adder" must be added to the respective AC parameter to determine worst-case timing.

FIG. 7 I_{CC} VS F_{MAX}

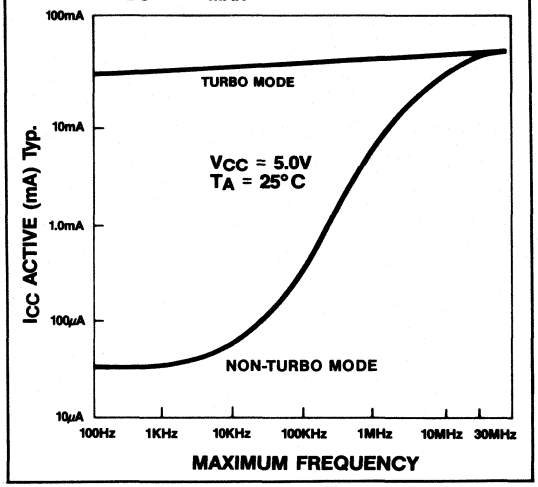
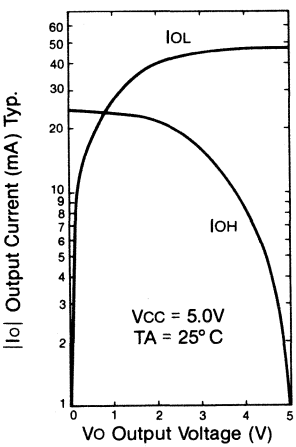


FIG. 8 OUTPUT DRIVE CURRENTS

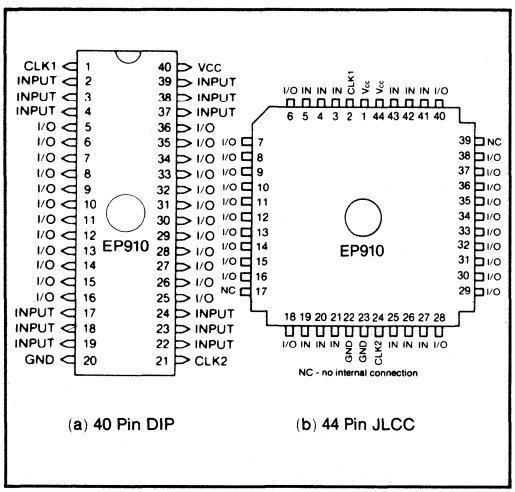


HIGH PERFORMANCE 24-MACROCELL EPLD — EP910

FEATURES

- High density logic replacement for TTL and 74HC.
- Functional and pin compatible with the Altera EP900.
- High speed, tpd = 30 ns.
- Asynchronous clocking of all registers or banked register operation from 2 synchronous clocks.
- 24 Macrocells with configurable I/O architecture allowing 36 inputs and 24 outputs.
- "Zero Power" (typically 20μA standby).
- Programmable registers providing D, T, SR or JK flipflops with individual Asynchronous Clear control.
- 100% generically testable—provides 100% programming yield.
- Programmable "Security Bit" allows total protection of proprietary designs.
- Package options include both a 40 pin, 600 mil DIP and a 44 pin J-leaded chip carrier.
- Full software support featuring Schematic Capture, Netlist, Boolean Equation and State Machine design entry methods.

CONNECTION DIAGRAM



(a) 40 Pin DIP (b) 44 Pin JLCC

PRELIMINARY DATA

NOTICE: THIS IS NOT A FINAL SPECIFICATION. SOME PARAMETRIC LIMITS ARE SUBJECT TO CHANGE.

GENERAL DESCRIPTION

The Altera EP910 is an enhanced performance, pin-compatible version of the popular EP900 Erasable Programmable Logic Device (EPLD). Available in 40-pin DIP and 44-pin J-leaded chip carrier packages, the EP910 contains 24 Macrocells with user-configurable I/O architecture, allowing up to 36 inputs and 24 outputs.

Each of the 24 Macrocells contains a programmable AND and fixed OR PLA structure, see Figure 1, with a maximum eight product terms for logic implementation. In addition, single product terms control Output Enable/Asynchronous Clock and Asynchronous Clear functions.

The Altera proprietary programmable I/O architecture allows the EP910 user to program output and feedback paths for both combinatorial or registered operation, active high or active low.

For increased flexibility, the EP910 also includes programmable registers. Each of the 24 internal registers may be programmed to be D, T, SR or JK flipflop. In addition, each register may be clocked asynchronously on an individual basis or synchronously on a banked register basis.

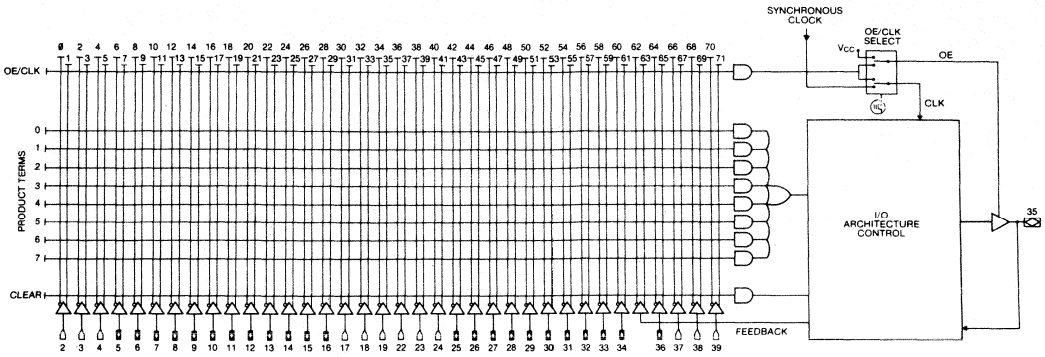
For proper operation, standard high performance design practices should be followed. It is recommended that opaque labels be placed over device window. Input and output pins must be constrained to the range GND $\leq$ (V_{IN} or V_{OUT}) $\leq$ V_{CC}. Unused inputs must always be tied to an appropriate logic level (e.g. either V_{CC} or GND). Each set of V_{CC} and GND pins must be shorted together directly at the device. Power supply decoupling capacitors of at least .2μF must be connected between each V_{CC} pin and GND. For the most effective decoupling, connect one capacitor between each set of V_{CC} and GND pins, directly at the device.

Programming the EP910 is accomplished by using the Altera A+PLUS PC-based development software which supports schematic capture, netlist, state machine and Boolean equation design entry methods. Once the design is entered, A+PLUS automatically performs translation into logical equations, Boolean minimization, and design fitting directly to an EP910. The device may then be programmed to achieve customized working silicon within minutes at the designer's own desktop.

For full EP910 functional description, please consult the EP900 datasheet.

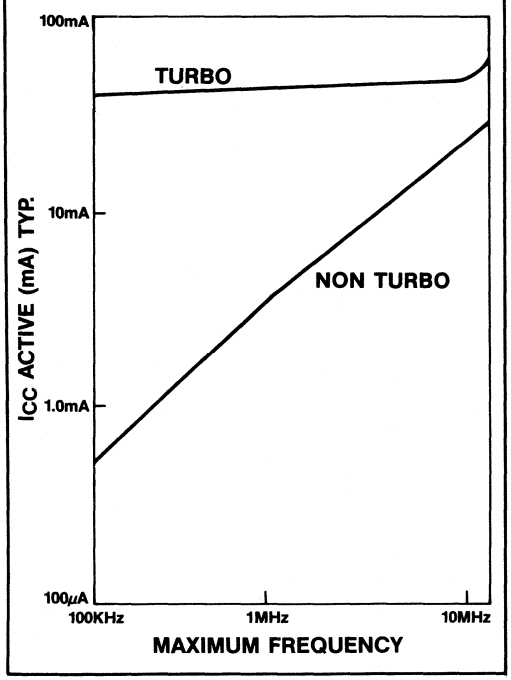
REV. 1.1

Figure 1. Logic Array Macrocell



*Note ◇ = I/O Pin, in which Logic Array input is from feedback path.
Pin numbers reflect 40 pin DIP.

Figure 2. I_{CC} vs. F_{MAX}



Note:
These preliminary specifications are provided for evaluation purposes. Conservative values are shown prior to full device characterization. Request a copy of the current EP910 Electrical Specification for complete information.

A Military Product Drawing will be prepared, in accordance with appropriate military specification formats, to provide guidance for the preparation of source control drawings (SCD).

ABSOLUTE MAXIMUM RATINGS

COMMERCIAL
OPERATING RANGE

Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	With respect to GND note (3)	-2.0	7.0	V
V_{PP}	Programming supply voltage		-2.0	13.5	V
V_I	DC INPUT voltage		-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		-200	+200	mA
I_{OUT}	DC OUTPUT current, per pin		-25	+25	mA
P_D	Power dissipation			1.0	W
T_{STG}	Storage temperature	No bias	-65	+150	°C
T_{AMB}	Ambient temperature	Under bias	-65	+135	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage		4.75	5.25	V
V_I	INPUT voltage		0	V_{CC}	V
V_O	OUTPUT voltage		0	V_{CC}	V
T_A	Operating temperature		0	70	°C
T_R	INPUT rise time	note (9)		500	ns
T_F	INPUT fall time	note (9)		500	ns

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)
Note (1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3		0.8	V
V_{OH}	HIGH level TTL output voltage	I_{OH} = -4mA DC	2.4			V
V_{OH}	HIGH level CMOS output voltage	I_{OH} = -2mA DC	3.84			V
V_{OL}	LOW level output voltage	I_{OL} = 4mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	-10		+10	μA
I_{OZ}	3-state output off-state current	V_O = V_{CC} or GND	-10		+10	μA
I_{CC1}	V_{CC} supply current (Non Turbo standby)	V_I = V_{CC} or GND I_O = 0 note (8)		20	100	μA
I_{CC2}	V_{CC} supply current (Non Turbo active)	V_I = V_{CC} or GND No load, f = 1.0MHz note (7)		15		mA
I_{CC3}	V_{CC} supply current (Turbo active)	V_I = V_{CC} or GND No load, f = 1.0MHz note (7)		60		mA

CAPACITANCE

Note (4)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1.0 MHz		20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1.0 MHz		20	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V f = 1.0 MHz		20	pF

AC CHARACTERISTICS Note (5)

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)

Note:
These are typical values derived from design simulations. Call Altera Applications or your local representative for the most recent values.

			EP910-30			EP910-35			EP910-40			
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
t_{PD1}	Input to non-registered output	C_1 = 35pF note (6)			30			35			40	ns
t_{PD2}	I/O input to non-registered output				32			37			42	ns
t_{PZX}	Input to output enable			25			30			35		ns
t_{PXZ}	Input to output disable	C_1 = 5pF note (2)		25			30			35		ns
t_{CLR}	Asynchronous output clear time	C_1 = 35pF		25			30			35		ns
t_{IO}	I/O input buffer delay			2			2			2		ns

SYNCHRONOUS CLOCK MODE

			EP910-30			EP910-35			EP910-40			
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
f_{MAX}	Maximum frequency	note (10)		50			44			37		MHz
t_{SU}	Input setup time			20			23			27		ns
t_H	Input hold time			0			0			0		ns
t_{CH}	Clock high time			10			12			13.5		ns
t_{CL}	Clock low time			10			12			13.5		ns
t_{CO1}	Clock to output delay			15			18			20		ns
t_{CNT}	Minimum clock period (register output feedback to register input - internal path)	note (7)		25			30			35		ns
f_{CNT}	Internal maximum frequency ($1/t_{CNT}$)	note (7)		40			33.3			28.6		MHz

ASYNCHRONOUS CLOCK MODE

			EP910-30			EP910-35			EP910-40			
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
f_{MAX}	Maximum frequency	note (10)		50			44			37		MHz
t_{ASU}	Input setup time			5			5			5		ns
t_{AH}	Input hold time			5			5			5		ns
t_{ACH}	Clock high time			10			12			13.5		ns
t_{ACL}	Clock low time			10			12			13.5		ns
t_{ACO1}	Clock to output delay			25			30			35		ns
t_{ACNT}	Minimum clock period (register output feedback to register input - internal path)	note (7)		25			30			35		ns
f_{ACNT}	Internal maximum frequency ($1/t_{ACNT}$)	note (7)		40			33.3			28.6		MHz

Notes:
1. Typical values are for T_A = 25°C, V_{CC} = 5V
2. Sample tested only for an output change of 500mV.
3. Minimum DC input is -0.3V. During transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
4. Capacitance measured at 25°C. Sample tested only. Clock pin capacitance for dedicated clock inputs only. Pin 21, high voltage pin during programming, has capacitance of 60pF max.
5. All AC values tested with TURBO-BIT™ programmed.
6. T_{PD} (NON TURBO) increases by 15ns.
7. Measured with device programmed as a 24 bit counter.
8. EPLD automatically goes into standby mode if logic transitions do not occur when in non-turbo mode (approximately 100ns after last transition).
9. Clock t_R, t_F = 100ns.
10. The f_{MAX} values shown represent the highest frequency for pipelined data.

ALTERA

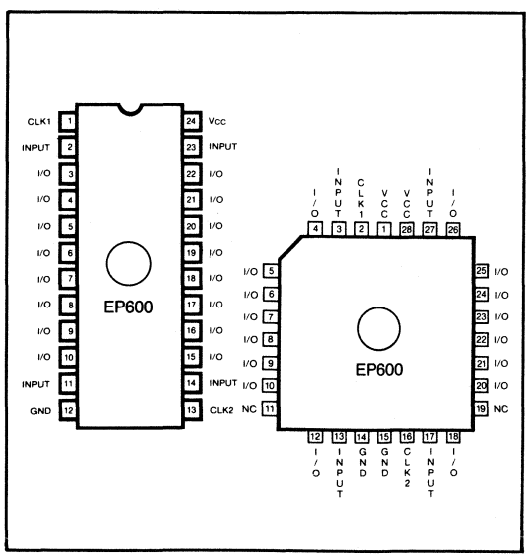
16 MACROCELL EPLD

EP600

FEATURES

- High density (over 600 gates) replacement for TTL and 74HC.
- Advanced CHMOS EPROM technology, allows erase and reprogram.
- High speed, t_{pd} = 45 ns.
- "Zero Power" (typically 10μA standby).
- Asynchronous clocking of all registers or banked register operation from 2 synchronous clocks.
- Sixteen Macrocells with configurable I/O architecture allowing 20 inputs and 16 outputs.
- Programmable registers providing D, T, SR or JK flipflops with individual Clear control.
- 100% generically testable—provides 100% programming yield.
- Programmable "Security Bit" allows total protection of proprietary designs.
- Advanced software support featuring Schematic Capture, Interactive Netlist, Boolean Equation and State Machine design entry.
- Space saving 24 pin, 300 mil, dual in-line package and 28 pin J-leaded chip carrier.

CONNECTION DIAGRAM



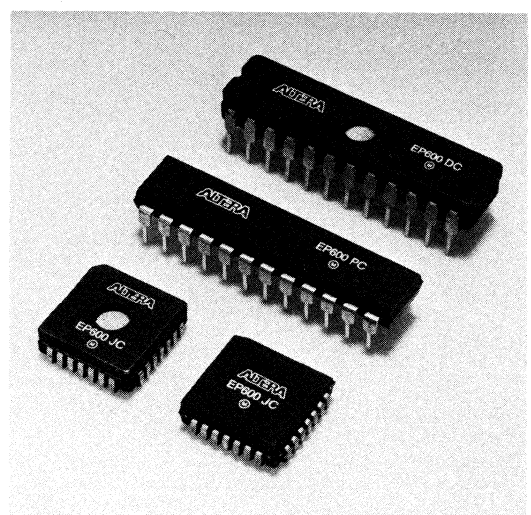
GENERAL DESCRIPTION

The ALTERA EP600 Programmable Logic Device is capable of implementing over 600 equivalent gates of SSI and MSI logic functions all in a space saving 24 pin, DIP, 300 mil package or a 28 pin J-leaded chip carrier.

The EP600 uses familiar sum-of-products logic providing a programmable AND with fixed OR structure. The device accommodates both combinatorial and sequential logic functions with up to 20 inputs and 16 outputs. The EP600 includes an ALTERA proprietary programmable I/O architecture providing individual selection of either combinatorial or registered output and feedback signals, active high or low.

A unique feature of the EP600 is the ability to program D, T, SR, or JK flipflop operation individually for each output without sacrificing product terms. In addition, each register can be individually clocked from any of the input or feedback paths available in the AND array. These features allow a variety of logic functions to be simultaneously implemented.

The CHMOS EPROM technology reduces the power consumption to less than 20% of equivalent bipolar devices without sacrificing speed performance. Other advantages include: 100% generic testing (all devices are 100% tested at the factory). The device can be erased with ultraviolet light. Design changes are no longer costly, nor is there a need for post programming testing.



REV. 4.0

ALTERA

Programming the EP600 is accomplished with the use of Altera's A+PLUS development software which supports four different design entry methods. Once the circuit has been entered, the A+PLUS software performs automatic translation into logical equations, boolean minimization, and design fitting directly into an EP600.

FUNCTIONAL DESCRIPTION

The EP600 is an Erasable Programmable Logic Device (EPLD) which uses a CMOS EPROM technology to configure connections in a programmable AND logic array. The device also contains a revolutionary programmable I/O architecture which provides advanced functional capability for user programmable logic.

Externally, the EP600 provides 4 dedicated data inputs, 2 synchronous clock inputs, and 16 I/O pins which may be configured for input, output, or bi-directional operation.

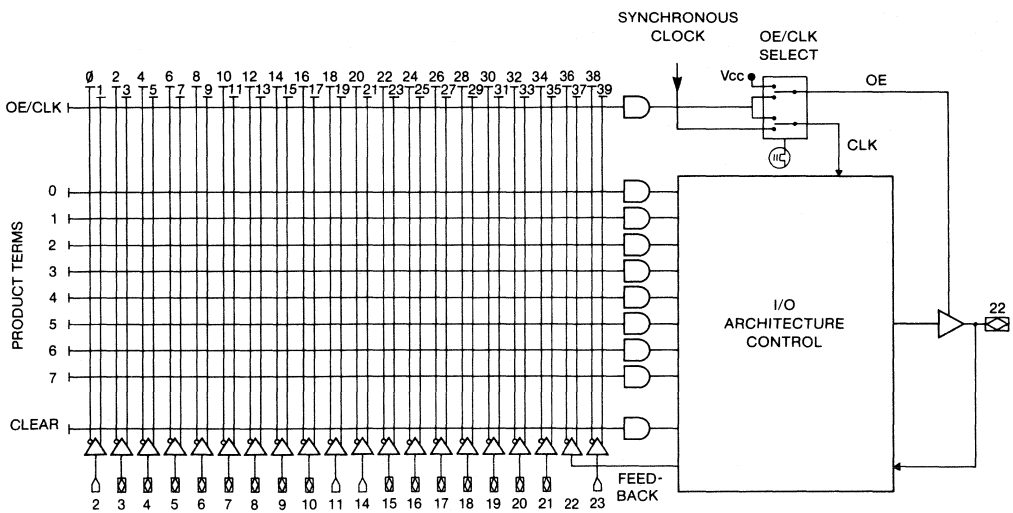
Figure 1 and 2 shows the EP600 basic Macrocell and the complete block diagram. The internal architecture is organized with familiar sum-of-products (AND-OR) structure. Inputs to the programmable AND array come from true and complement signals of the four dedicated data inputs and sixteen I/O architecture control blocks. The 40 input AND array encompasses 160 product terms which are distributed among 16 available Macrocells. Each EP600 product term represents a 40 input AND gate.

Each Macrocell contains ten product terms. Eight product terms are dedicated for logic implementation. One product term is used for Clear control of the Macrocell internal register. The remaining product term is used for Output Enable/Asynchronous Clock implementation.

At the intersection point of an input signal and a product term there exists an EPROM connection. In the erased state, all connections are made. This means both the true and complement of all inputs are connected to each product term. Connections are opened during the programming process. Therefore, any product term may be connected to the true or complement of any array input signal. When both the true and complement of any signal is left intact, a logical false results on the output of the AND gate. If both the true and complement connections are open, then a logical "don't care" results for that input. If all inputs for the product term are programmed open, then a logical true results on the output of the AND gate.

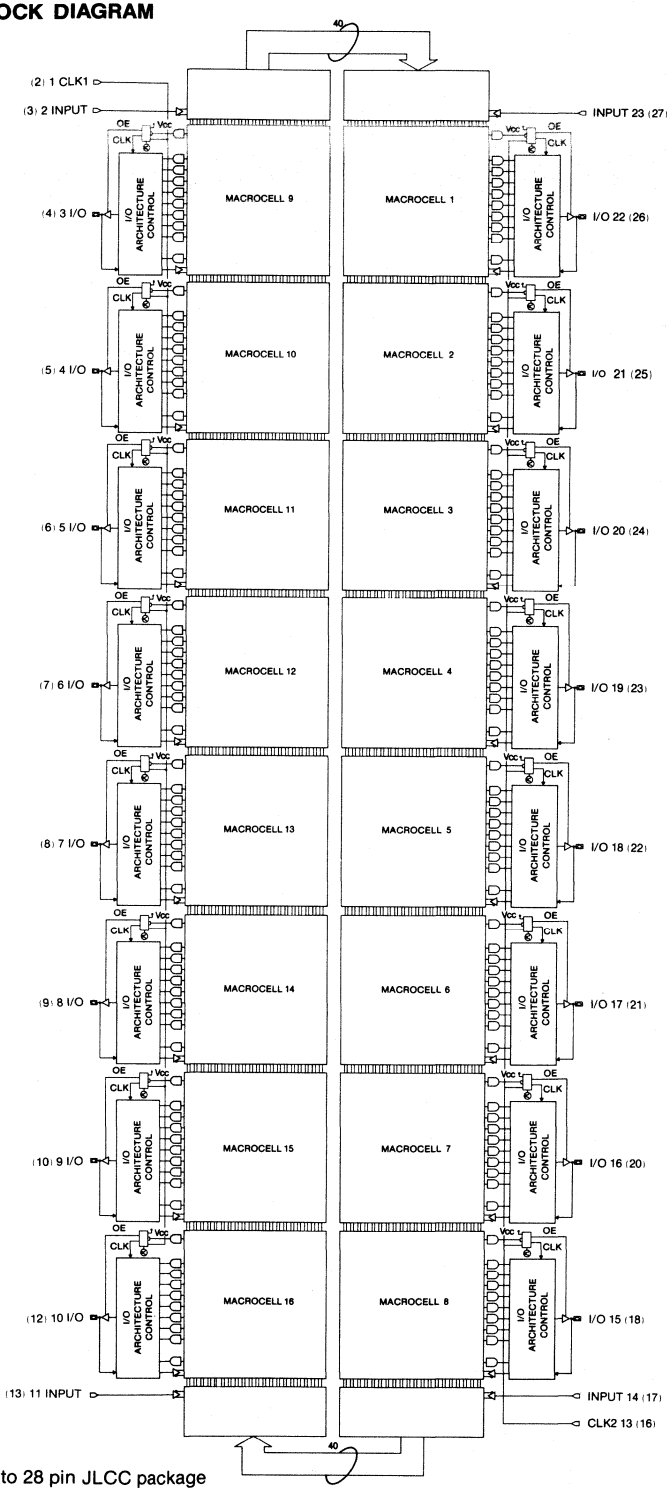
Two dedicated clock inputs provide synchronous clock signals to the EP600 internal registers. Each of the clock signals controls a bank of eight registers. CLK1 controls registers associated with Macrocells 9-16. CLK2 controls registers associated with Macrocells 1-8. The EP600 advanced I/O architecture allows the number of synchronous registers to be user defined, from one to sixteen. Both dedicated clock inputs are positive edge triggered.

FIG. 1 LOGIC ARRAY MACROCELL



Note: ◇ = I/O pin, in which Logic Array input is from feedback path.

FIG. 2 EP600 BLOCK DIAGRAM



Pin #'s in ( ) pertain to 28 pin JLCC package

ALTERA

I/O ARCHITECTURE

The EP600 Input/Output Architecture provides each Macrocell with over 50 possible I/O configurations. Each I/O can be configured for combinatorial or registered output, with programmable output polarity. Four different types of registers (D, T, JK, SR), can be implemented into every I/O without any additional logic requirements. I/O feedback selection can also be programmed for registered or input (pin) feedback. Another benefit of the EP600 I/O architecture is its ability to individually clock each internal register from asynchronous clock signals.

OE/CLK Selection

Figure 3 shows the two modes of operation which are provided by the OE/CLK Select Multiplexer. The operation of this multiplexer is controlled by a single EPROM bit and may be individually configured for each EP600 I/O pin. In Mode 0, the three-state output buffer is controlled by a single product term. If the output of the AND gate is a logical true then the output buffer is enabled. If a logical false resides on the output of the AND gate then the output buffer is seen as high impedance. In this mode the Macrocell flipflop may be clocked by its respective synchronous clock input. After erasure, OE/CLK Select Mux is configured as Mode 0.

In Mode 1, the Output Enable buffer is always enabled. The Macrocell flipflop now may be triggered from an asynchronous clock signal generated by the OE/CLK multiplexable product term. This mode allows individual clocking of flipflops from any available signal in the AND array. Because both true and complement signals reside in the AND array, the flipflop may be configured for positive or negative edge trigger operation. With the clock now controlled by a product term, gated clock structures are also possible.

OUTPUT/FEEDBACK Selection

Figure 4 shows the EP600 basic output configurations. Along with combinatorial output, four register types are available. Each Macrocell I/O may be independently configured. All registers have individual Asynchronous Clear control from a dedicated product term. When the product term is asserted to a logical one, the Macrocell register will immediately be loaded with a logical zero independently of the clock. On power up, the EP600 performs the Clear function automatically.

When the D or T register is selected, eight product terms are ORed together and made available to the register input. The Invert Select EPROM bit determines output polarity. The Feedback Select Multiplexer enables registered, I/O (pin) or no feedback to the AND array.

If the JK or SR registers are selected, the eight product terms are shared among two OR gates. The allocation of product terms for each register input is optimized by the A+PLUS development software. The Invert Select EPROM bits configures output polarity. The Feedback Select Multiplexer enables registered or no feedback to the AND array.

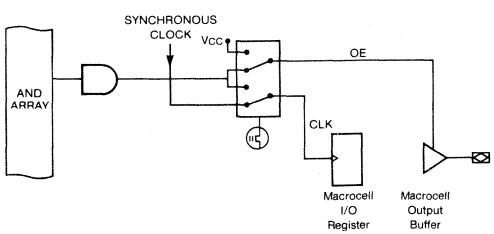
Any I/O pin may be configured as a dedicated input by selecting no output and pin feedback. No output is obtained by disabling the Macrocell output buffer.

In the erased state, the I/O is configured for combinatorial active low output with input (pin) feedback.

FIG. 3 OE/CLK SELECT MUX

MODE Ø

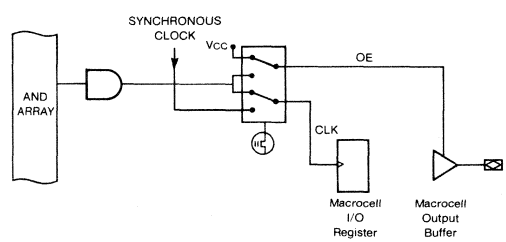
OE = P-Term Controlled
CLK = Synchronous



The register is clocked by the synchronous clock signal which is common to 7 other Macrocells. The output is enabled by the logic from the product term.

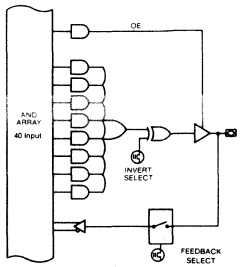
MODE 1

OE = Enabled
CLK = Asynchronous



The output is permanently enabled and the register is clocked via the product term. This allows for gated clocks that may be generated from elsewhere in the EP600.

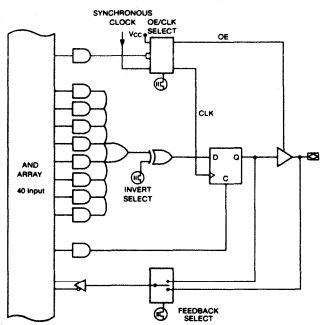
FIG. 4 I/O CONFIGURATIONS



COMBINATORIAL

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
Combinatorial/High	Pin, None
Combinatorial/Low	Pin, None
None	Pin



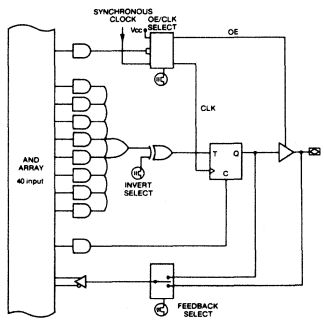
D-TYPE FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
D-Register/High	D-Register, Pin, None
D-Register/Low	D-Register, Pin, None
None	D-Registered
None	Pin

FUNCTION TABLE

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1



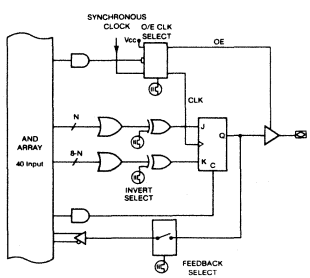
TOGGLE FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
T-Register / High	T-Register, Pin, None
T-Register / Low	T-Register, Pin, None
None	T-Register
None	Pin

FUNCTION TABLE

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0



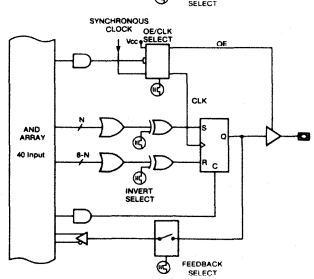
JK FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
JK Register/High	JK Register, None
JK Register/Low	JK Register, None
None	JK Register

FUNCTION TABLE

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



SR FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
SR Register/High	SR Register, None
SR Register/Low	SR Register, None
None	SR Register

FUNCTION TABLE

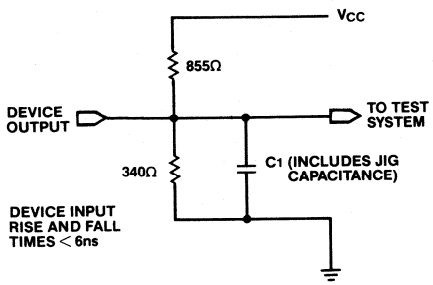
S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1

FUNCTIONAL TESTING

The EP600 is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

As a result, traditional problems associated with fuse-programmed circuits are eliminated. The erasable nature of the EP600 allows test program patterns to be used and then erased. This facility to use application-independent, general purpose tests is called generic testing and is unique among user-defined LSI logic devices.

FIG. 6 AC TEST CONDITIONS



Power supply transients can affect AC measurements, simultaneous transitions of multiple outputs should be avoided for accurate measurement. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

DESIGN SECURITY

The EP600 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied nor retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

TURBO-BIT

Some EPLDs contain a programmable option to control the automatic power down feature that enables the low standby power mode of the device. This option is controlled by a TURBO-BIT which can be set using A+PLUS. When the TURBO-BIT is programmed (Turbo = ON), the low standby power mode (Icc1) is disabled. This renders the circuit less sensitive to Vcc noise transients which can be created by the power-up/power-down cycle when operating in the low power mode. The typical Icc vs frequency data for both Turbo and Non-Turbo (low power) mode is shown in each EPLD data sheet. All AC values are tested with the TURBO-BIT programmed.

If the design requires low power operation then the TURBO-BIT should be disabled (Turbo = OFF). When operating in this mode, some AC parameters are subject to increase. Values given in the AC specifications section under "Non-Turbo Adder" must be added to the respective AC parameter to determine worst-case timing.

FIG. 7 I_{CC} VS F_{MAX}

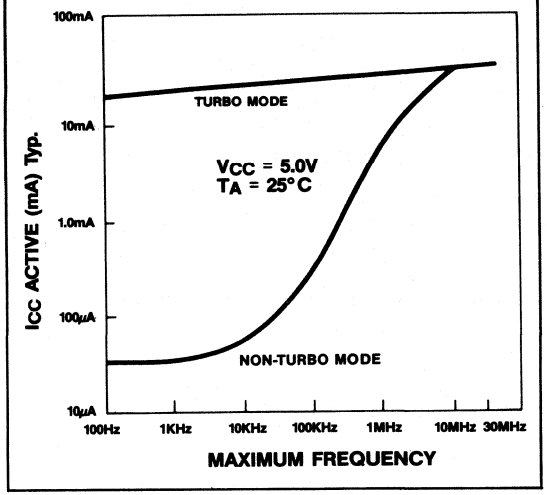
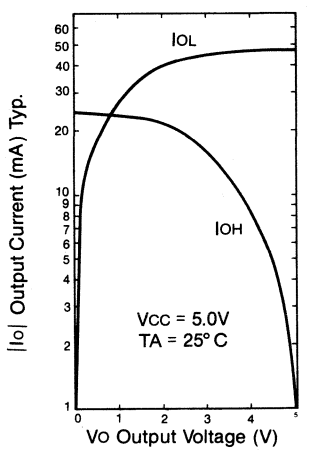


FIG. 8 OUTPUT DRIVE CURRENTS



ABSOLUTE MAXIMUM RATINGS

Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	With respect to GND note (3)	-2.0	7.0	V
V_{PP}	Programming supply voltage		-2.0	13.5	V
V_I	DC INPUT voltage		-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		-100	+100	mA
I_{OUT}	DC OUTPUT current, per pin		-25	+25	mA
P_D	Power dissipation			500	mW
T_{STG}	Storage temperature	No bias	-65	+150	°C
T_{AMB}	Ambient temperature	Under bias	-65	+135	°C
ESD	ElectroStatic Discharge Voltage		±2100		V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage	note (6)	4.75 (4.5)	5.25 (5.5)	V
V_I	INPUT voltage		0	V_{CC}	V
V_O	OUTPUT voltage		0	V_{CC}	V
T_A	Operating temperature	For Commercial	0	70	°C
T_A	Operating temperature	For Industrial	-40	85	°C
T_C	Case temperature	For Military	-55	125	°C
T_R	INPUT rise time	note (9)		500	ns
T_F	INPUT fall time	note (9)		500	ns

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = 0° C to 70° C for Commercial)
(V_{CC} = 5V ± 10%, T_A = -40° C to 85° C for Industrial)
(V_{CC} = 5V ±10%, T_C = -55° C to 125° C for Military)*
Note (1) and (6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3		0.8	V
V_{OH}	HIGH level TTL output voltage	I_{OH} = -4mA DC	2.4			V
V_{OH}	HIGH level CMOS output voltage	I_{OH} = -2mA DC	3.84			V
V_{OL}	LOW level output voltage	I_{OL} = 4mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	-10		+10	µA
I_{OZ}	3-state output off-state current	V_O = V_{CC} or GND	-10		+10	µA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND No load note (8)		35	150	µA
I_{CC2}	V_{CC} supply current (non-turbo)	V_I = V_{CC} or GND No load, f = 1.0 MHz note (7)		3	10 (15)	mA
I_{CC3}	V_{CC} supply current (turbo)	V_I = V_{CC} or GND No load, f = 1.0 MHz note (7)		30	50 (60)	mA

CAPACITANCE

Note (4)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1.0 MHz		20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1.0 MHz		20	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V f = 1.0 MHz		20	pF

AC CHARACTERISTICS Note (5)

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)
(V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial)
(V_{CC} = 5V ± 10%, T_C = -55°C to 125°C for Military)*

			EP600-3		EP600		NON-TURBO ADDER (note 5)		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t_{PD1}	Input to non-registered output	C_1 = 50pF		43		53		25	ns
t_{PD2}	I/O input to non-registered output			45		55		25	ns
t_{PZX}	Input or I/O input to output enable			45		55		25	ns
t_{PXZ}	Input or I/O input to output disable	C_1 = 5pF note (2)		45		55		25	ns
t_{CLR}	Asynchronous output clear time	C_1 = 50pF		45		55		25	ns
t_{IO}	I/O input buffer delay			2		2		0	ns

SYNCHRONOUS CLOCK MODE

			EP600-3		EP600		NON-TURBO ADDER		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
f_{MAX}	Maximum frequency		26.3		23.3		0		MHz
t_{SU}	Input or I/O input setup time		38		43		25		ns
t_H	Input or I/O input hold time		0		0		0		ns
t_{CH}	Clock high time		17.5		21.5		0		ns
t_{CL}	Clock low time		17.5		21.5		0		ns
t_{CO1}	Clock to output delay			22		25		0	ns
t_{CNT}	Minimum clock period (register output feedback to register input - internal path)	note (7)		45		55		0	ns
f_{CNT}	Internal maximum frequency ($1/t_{CNT}$)	note (7)	22.2		18.2		0		MHz

ASYNCHRONOUS CLOCK MODE

			EP600-3		EP600		NON-TURBO ADDER		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
f_{MAX}	Maximum frequency		26.3		23.3		0		MHz
t_{ASU}	Input or I/O input setup time		10		10		25		ns
t_{AH}	Input or I/O input hold time		15		15		0		ns
t_{ACH}	Clock high time		17.5		21.5		0		ns
t_{ACL}	Clock low time		17.5		21.5		0		ns
t_{ACO1}	Clock to output delay			50		58		25	ns
t_{ACNT}	Minimum clock period (register output feedback to register input - internal path)			45		55		0	ns
f_{ACNT}	Internal maximum frequency ($1/t_{ACNT}$)		22.2		18.2		0		MHz

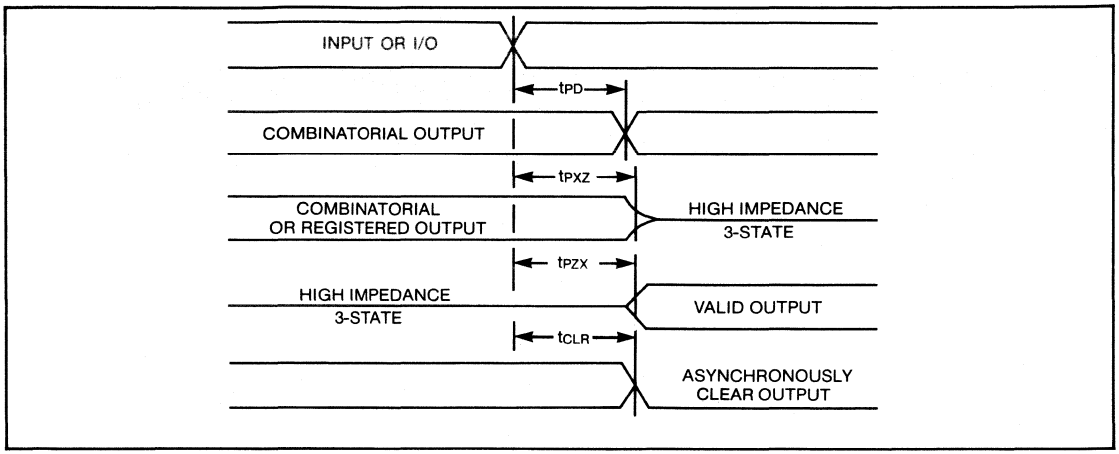
Notes:
1. Typical values are for T_A = 25°C, V_{CC} = 5V
2. Sample tested only for an output change of 500mV.
3. Minimum DC input is -0.3V. During transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
4. Capacitance measured at 25°C. Sample tested only. Clock pin capacitance for dedicated clock inputs only. Pin 13, (high voltage pin during programming), has capacitance of 50 pF max.
5. See TURBO-BIT™, page 2-43.
6. Figures in ( ) pertain to military temperature version.
7. Measured with device programmed as a 16 bit counter.
8. EPLD automatically goes into standby mode if logic transitions do not occur when in non-turbo mode (approximately 100 ns after last transition).
9. Clock t_R, t_F = 250ns (100ns).
10. The f_{MAX} values shown represent the highest frequency for pipelined data.

GRADE	AVAILABILITY
Commercial (0°C to 70°C)	EP600-3 EP600
Industrial (-40°C to 85°C)	EP600-3 EP600
Military (-55°C to 125°C)	EP600

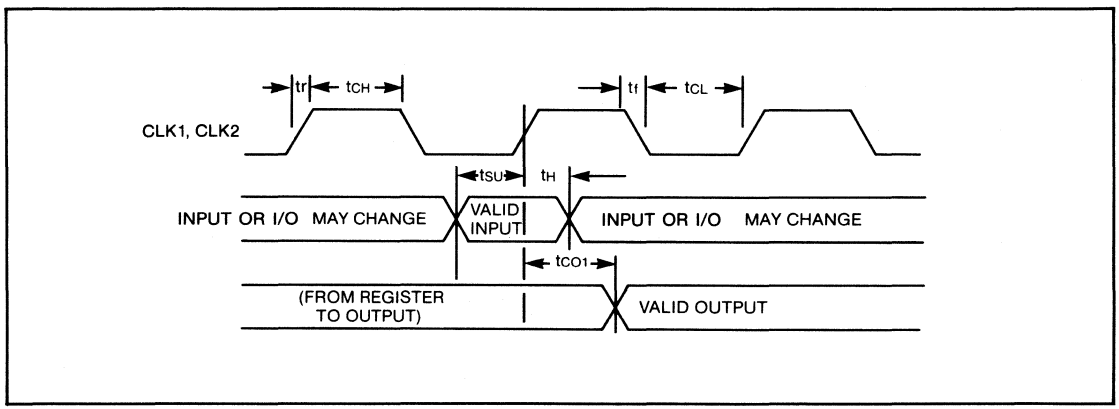
*** Specifications for MIL-STD-883 device may vary from those above. A Military Product Drawing, prepared in accordance with appropriate military specification formats, is available to provide guidance for the preparation of Source Control Drawings (SCD). Please contact Altera Marketing at (408) 984-2800 x 101 to obtain 883 Product drawings.**

FIG. 5 SWITCHING WAVEFORMS

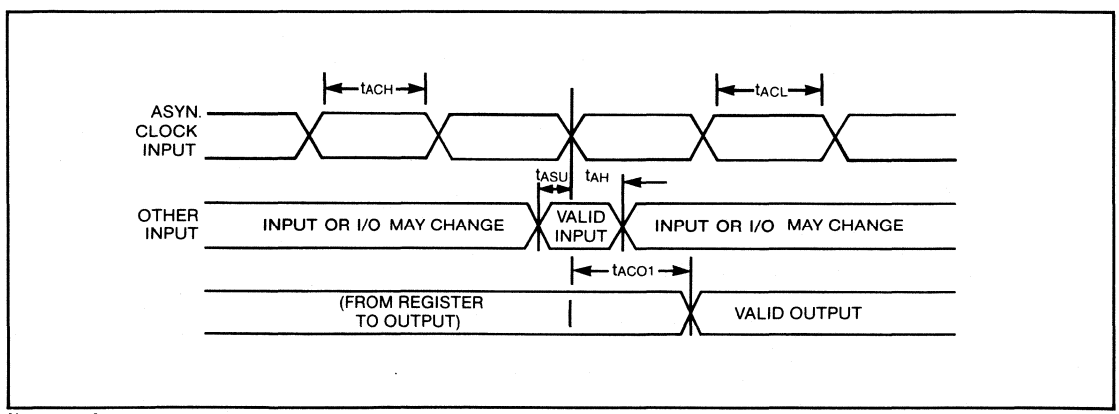
COMBINATORIAL MODE



SYNCHRONOUS CLOCK MODE



ASYNCHRONOUS CLOCK MODE



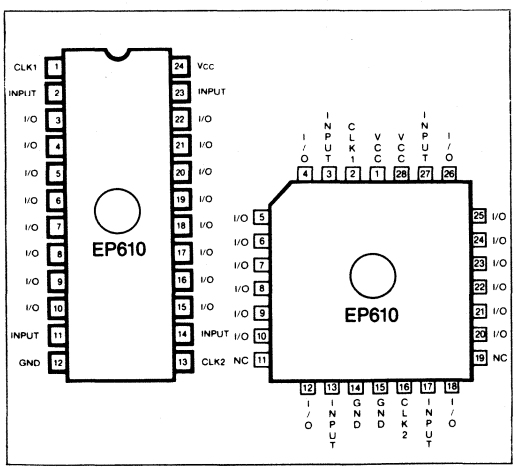
Notes: tr & tf < 6ns
tCL & tCH measured at 0.3V and 2.7V
all other timing at 1.5V
Input voltage levels at ϕV and 3V

HIGH PERFORMANCE 16-MACROCELL EPLD — EP610

FEATURES

- High density logic replacement for TTL and 74HC.
- Functional and pin compatible with the Altera EP600.
- High speed, tpd = 25 ns.
- Asynchronous clocking of all registers or banked register operation from 2 synchronous clocks.
- 16 Macrocells with configurable I/O architecture allowing 20 inputs and 16 outputs.
- "Zero Power" (typically 20μA standby).
- Programmable registers providing D,T,SR or JK flipflops with individual Asynchronous Clear control.
- 100% generically testable-provides 100% programming yield.
- Programmable "Security Bit" allows total protection of proprietary designs.
- Package options include both a 24 pin, 300 mil DIP and a 28 pin J-leaded chip carrier.
- Full software support featuring Schematic Capture, Netlist, Boolean Equation and State Machine design entry methods.

CONNECTION DIAGRAM



PRELIMINARY DATA

NOTICE: THIS IS NOT A FINAL SPECIFICATION. SOME PARAMETRIC LIMITS ARE SUBJECT TO CHANGE.

GENERAL DESCRIPTION

The Altera EP610 is an enhanced performance, pin-compatible version of the popular EP600 Erasable Programmable Logic Device (EPLD). Available in 24-pin DIP and 28-pin J-leaded chip carrier packages, the EP610 contains 16 Macrocells with user-configurable I/O architecture, allowing up to 20 inputs and 16 outputs.

Each of the 16 Macrocells contains a programmable AND and fixed OR PLA structure, see Figure 1, with a maximum eight product terms for logic implementation. In addition, single product terms control Output Enable/Asynchronous Clock and Asynchronous Clear functions.

The Altera proprietary programmable I/O architecture allows the EP610 user to program output and feedback paths for both combinatorial or registered operation, active high or active low.

For increased flexibility, the EP610 also includes programmable registers. Each of the 16 internal registers may be programmed to be D, T, SR or JK flipflop. In addition, each register may be clocked asynchronously on an individual basis or synchronously on a banked register basis.

For proper operation, standard high performance design practices should be followed. It is recommended that opaque labels be placed over device window. Input and output pins must be constrained to the range GND $\leq$ (V_{IN} or V_{OUT}) $\leq$ V_{CC}. Unused inputs must always be tied to an appropriate logic level (e.g. either V_{CC} or GND). Each set of V_{CC} and GND pins must be shorted together directly at the device. Power supply decoupling capacitors of at least .1μF must be connected between each V_{CC} pin and GND. For the most effective decoupling, connect one capacitor between each set of V_{CC} and GND pins, directly at the device.

Programming the EP610 is accomplished by using the Altera A+PLUS PC-based development software which supports schematic capture, netlist, state machine and Boolean equation design entry methods. Once the design is entered, A+PLUS automatically performs translation into logical equations, Boolean minimization, and design fitting directly to an EP610. The device may then be programmed to achieve customized working silicon within minutes at the designer's own desktop.

For full EP610 functional description please consult the EP600 datasheet.

REV. 1.1

ABSOLUTE MAXIMUM RATINGS

COMMERCIAL
OPERATING RANGE

Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	With respect to GND note (3)	-2.0	7.0	V
V_{PP}	Programming supply voltage		-2.0	13.5	V
V_I	DC INPUT voltage		-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		-200	+200	mA
I_{OUT}	DC OUTPUT current, per pin		-25	+25	mA
P_D	Power dissipation			1.0	W
T_{STG}	Storage temperature	No bias	-65	+150	°C
T_{AMB}	Ambient temperature	Under bias	-65	+135	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage		4.75	5.25	V
V_I	INPUT voltage		0	V_{CC}	V
V_O	OUTPUT voltage		0	V_{CC}	V
T_A	Operating temperature		0	70	°C
T_R	INPUT rise time	note (9)		500	ns
T_F	INPUT fall time	note (9)		500	ns

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)
Note (1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3		0.8	V
V_{OH}	HIGH level TTL output voltage	I_{OH} = -4mA DC	2.4			V
V_{OH}	HIGH level CMOS output voltage	I_{OH} = -2mA DC	3.84			V
V_{OL}	LOW level output voltage	I_{OL} = 4mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	-10		+10	μA
I_{OZ}	3-state output off-state current	V_O = V_{CC} or GND	-10		+10	μA
I_{CC1}	V_{CC} supply current (Non Turbo standby)	V_I = V_{CC} or GND I_O = 0 note (8)		20	100	μA
I_{CC2}	V_{CC} supply current (Non Turbo active)	V_I = V_{CC} or GND No load, f = 1.0MHz note (7)		3		mA
I_{CC3}	V_{CC} supply current (Turbo active)	V_I = V_{CC} or GND No load, f = 1.0MHz note (7)		32		mA

CAPACITANCE

Note (4)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1.0 MHz		20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1.0 MHz		20	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V f = 1.0 MHz		20	pF

AC CHARACTERISTICS Note (5)

EP610-25, EP610-30, EP610-35

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)

Note:
These are typical values derived from design simulations. Call Altera Applications or your local representative for the most recent values.

			EP610-25			EP610-30			EP610-35			
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
t_{PD1}	Input to non-registered output	C_1 = 35pF note (6)			25			30			35	ns
t_{PD2}	I/O input to non-registered output				27			32			37	ns
t_{PZX}	Input to output enable			22			26			30		ns
t_{PXZ}	Input to output disable	C_1 = 5pF note (2)		22			26			30		ns
t_{CLR}	Asynchronous output clear time	C_1 = 35pF		22			26			30		ns
t_{IO}	I/O input buffer delay			2			2			2		ns

SYNCHRONOUS CLOCK MODE

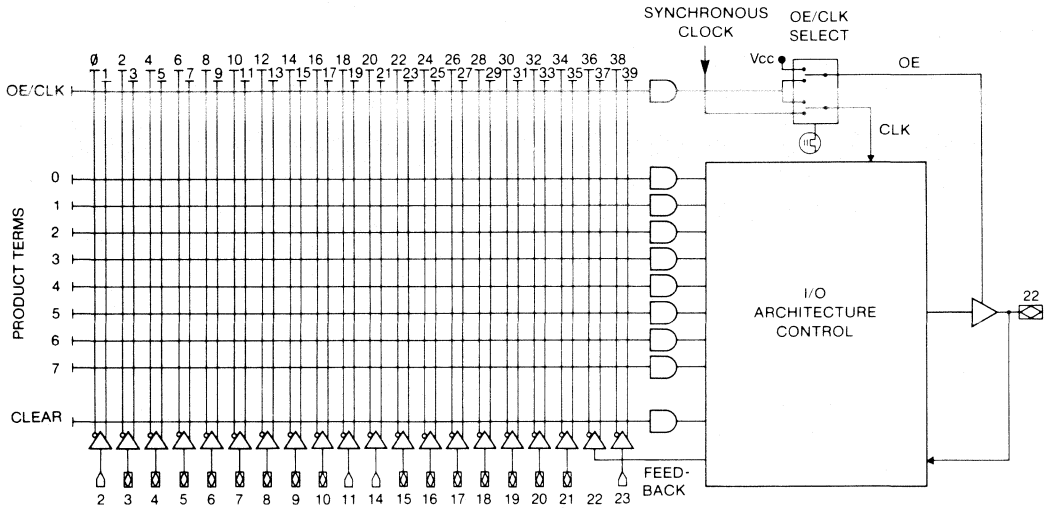
			EP610-25			EP610-30			EP610-35			
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
f_{MAX}	Maximum frequency	note (10)		66.7			53.4			40		MHz
t_{SU}	Input setup time			15			20			25		ns
t_H	Input hold time			0			0			0		ns
t_{CH}	Clock high time			7.5			10.0			12.5		ns
t_{CL}	Clock low time			7.5			10.0			12.5		ns
t_{CO1}	Clock to output delay			13			15.5			18		ns
t_{CNT}	Minimum clock period (register output feedback to register input - internal path)	note (7)		22			26			30		ns
f_{CNT}	Internal maximum frequency ($1/t_{CNT}$)	note (7)		45.5			39.3			33		MHz

ASYNCHRONOUS CLOCK MODE

			EP610-25			EP610-30			EP610-35			
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
f_{MAX}	Maximum frequency	note (10)		66.7			53.4			40		MHz
t_{ASU}	Input setup time			6			6			6		ns
t_{AH}	Input hold time			6			6			6		ns
t_{ACH}	Clock high time			7.5			10.0			12.5		ns
t_{ACL}	Clock low time			7.5			10.0			12.5		ns
t_{ACO1}	Clock to output delay			22			26			30		ns
t_{ACNT}	Minimum clock period (register output feedback to register input - internal path)	note (7)		22			26			30		ns
f_{ACNT}	Internal maximum frequency ($1/t_{ACNT}$)	note (7)		45.5			39.3			33		MHz

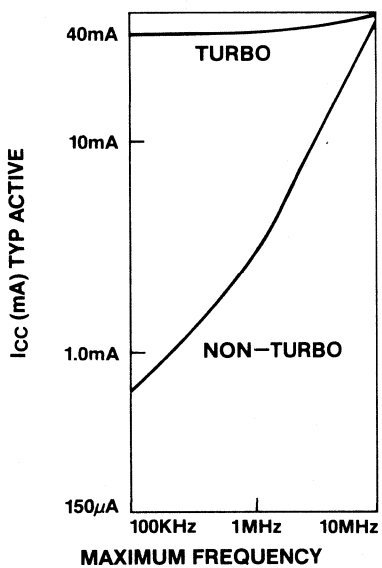
Notes:
1. Typical values are for T_A = 25°C, V_{CC} = 5V
2. Sample tested only for an output change of 500mV.
3. Minimum DC input is -0.3V. During transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
4. Capacitance measured at 25°C. Sample tested only. Clock pin capacitance for dedicated clock inputs only. Pin 13, high voltage pin during programming, has capacitance of 50pF max.
5. All AC values tested with TURBO-BIT™ programmed.
6. T_{PD} (NON TURBO) increases by 15ns.
7. Measured with device programmed as a 16 bit counter.
8. EPLD automatically goes into standby mode if logic transitions do not occur when in non-turbo mode (approximately 100ns after last transition).
9. Clock t_R, t_F = 100ns.
10. The f_{MAX} values shown represent the highest frequency for pipelined data.

Figure 1 Logic Array Macrocell



Note: ◇ = I/O pin, in which Logic Array input is from feedback path.

Figure 2. I_{CC} vs Frequency



Note:

These preliminary specifications are provided for evaluation purposes. Conservative values are shown prior to full device characterization. Request a copy of the current EP610 Electrical Specification for complete information.

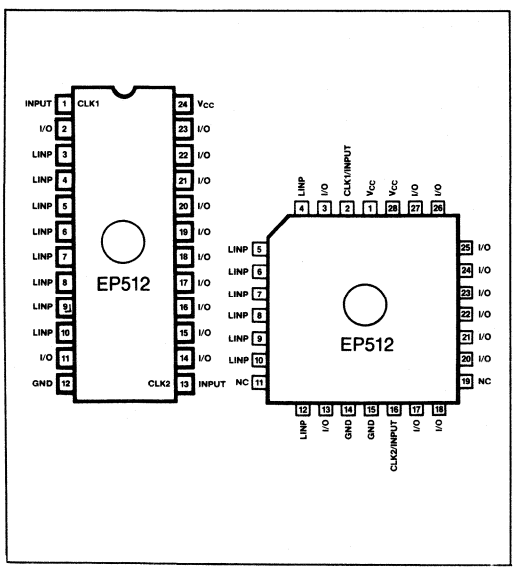
A Military Product Drawing will be prepared, in accordance with appropriate military specification formats, to provide guidance for the preparation of source control drawings (SCD).

HIGH PERFORMANCE 12-MACROCELL EPLD — EP512

FEATURES

- High performance LSI replacement for TTL and 74HC SSI and MSI logic.
- Advanced CMOS EPROM technology, allows erase and reprogram.
- High speed, tpd = 25 ns, and 40 MHz operating frequency.
- Programmable power option for 150 μA "stand-by" operation.
- Twelve Macrocells with configurable I/O architecture allowing up to 22 inputs (10 dedicated, 12 I/O) and 12 outputs.
- Eight programmable inputs which can be individually configured to implement latch, register, or flow-through mode; synchronous or asynchronous.
- Programmable product term allocation allowing up to 16 product terms for a single Macrocell.
- Two product tems for all Macrocell control logic (OE, Preset, Clear and Clock).
- Dual feedback on all Macrocells for buried register implementation and input usage.
- Advanced software support featuring Schematic Capture, Netlist, Boolean Equation and State Machine design entry.
- Space savings 24 pin DIP, 300 mil, and 28 pin JLCC/PLCC packages.
- Alternate sourced by Intel as the 5AC312.

CONNECTION DIAGRAM



GENERAL DESCRIPTION

The Altera EP512 EPLD (Erasable Programmable Logic Device) represents an innovative approach to PLD architecture. With an advanced I/O and Macrocell structure, the EP512 is capable of implementing high performance logic functions more effectively than previously possible. It can be used as an alterantive to low-end gate arrays, multiple programmable logic devices, or LS, HC- or HCT SSI and MSI logic devices.

The EP512 uses familiar sum of products logic providing a programmable AND with a fixed OR structure. The device can implement both combinatorial and sequential logic functions, active high or low. The EP512 contains a total of 12 I/O Macrocells, 8 user-configurable input structures (input register or flow-through operation) and 2 inputs that can be programmed to serve as either combinatorial inputs or clock inputs for the input and output register functions.

The EP512 macrocell contains a number of significant functional enhancements. Each macrocell contains 8 product terms for general purpose logic. Product terms may be re-allocated between adjacent macrocells yielding up to 16 product terms for a single macrocell. In addition, each macrocell contains two dedicated product terms for each control signal: OE, Preset, Clear, and Asynchronous Clock. All macrocells contain dual feedback allowing buried logic functions and at the same time serve as dedicated inputs.

The EP512 uses advanced CMOS EPROM cells as logic control elements instead of poly-silicon fuses. This technology allows the EP512 to operate in high performance applications while significantly reducing the power consumption. Other advantages include: 100% generic testing (all devices are 100% tested at the factory). The device can be erased with ultraviolet light. Design changes are no longer costly, nor is there a need for post programming testing.

ADVANCED INFORMATION

SPECIFICATIONS SUBJECT TO CHANGE

REV. 1.0


PLSLIB-TTL
Standard TTL
Macrofunction
Library
ALTERA
EP 1800 GC

ALTERA

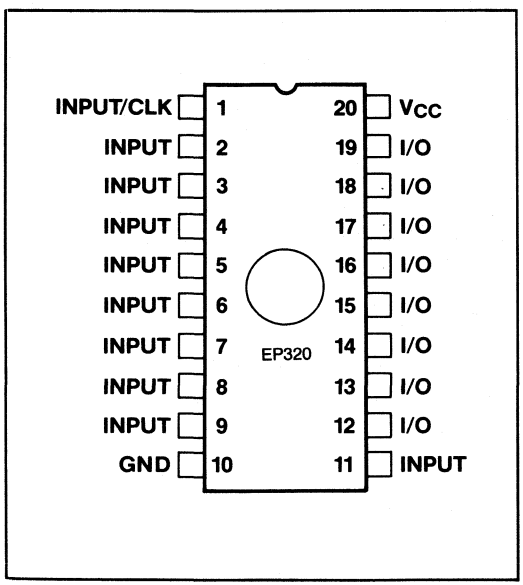
8 MACROCELL EPLD

EP320

FEATURES

- User-Configurable replacement for TTL, 74HC and 20 pin PAL Family.
- Advanced CMOS EPROM technology allows erase and reprogram.
- "Zero Power" (typically 10μA standby).
- High speed, tpd = 30ns.
- User-Configurable I/O architecture allows output and feedback paths to be configured for registered or combinatorial modes, active high or active low.
- 100% generically testable—provides 100% programming yield.
- Programmable "Security Bit" allows total protection of proprietary designs.
- Advanced software support allows convenience of 4 different design entry methods, complete Boolean minimization and automatic fitting into an EP320.

CONNECTION DIAGRAM



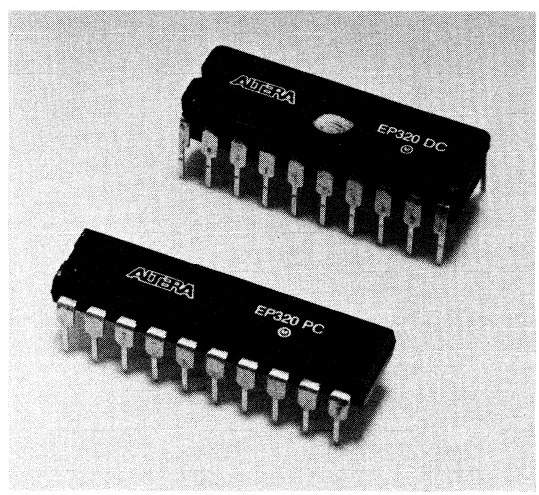
GENERAL DESCRIPTION

The ALTERA EP320 Erasable Programmable Logic Device may be used as a replacement for TTL and 74HC. It also provides a high speed, low power "plug compatible" replacement for fuse-based programmable logic devices.

The EP320 can accommodate up to 18 inputs and up to 8 outputs. The 20 pin, 300 mil package contains 8 Macrocells, each of which utilizes a programmable AND fixed OR structure. This AND-OR structure yields 8 product terms for the logic function as well as an individual product term for Output Enable.

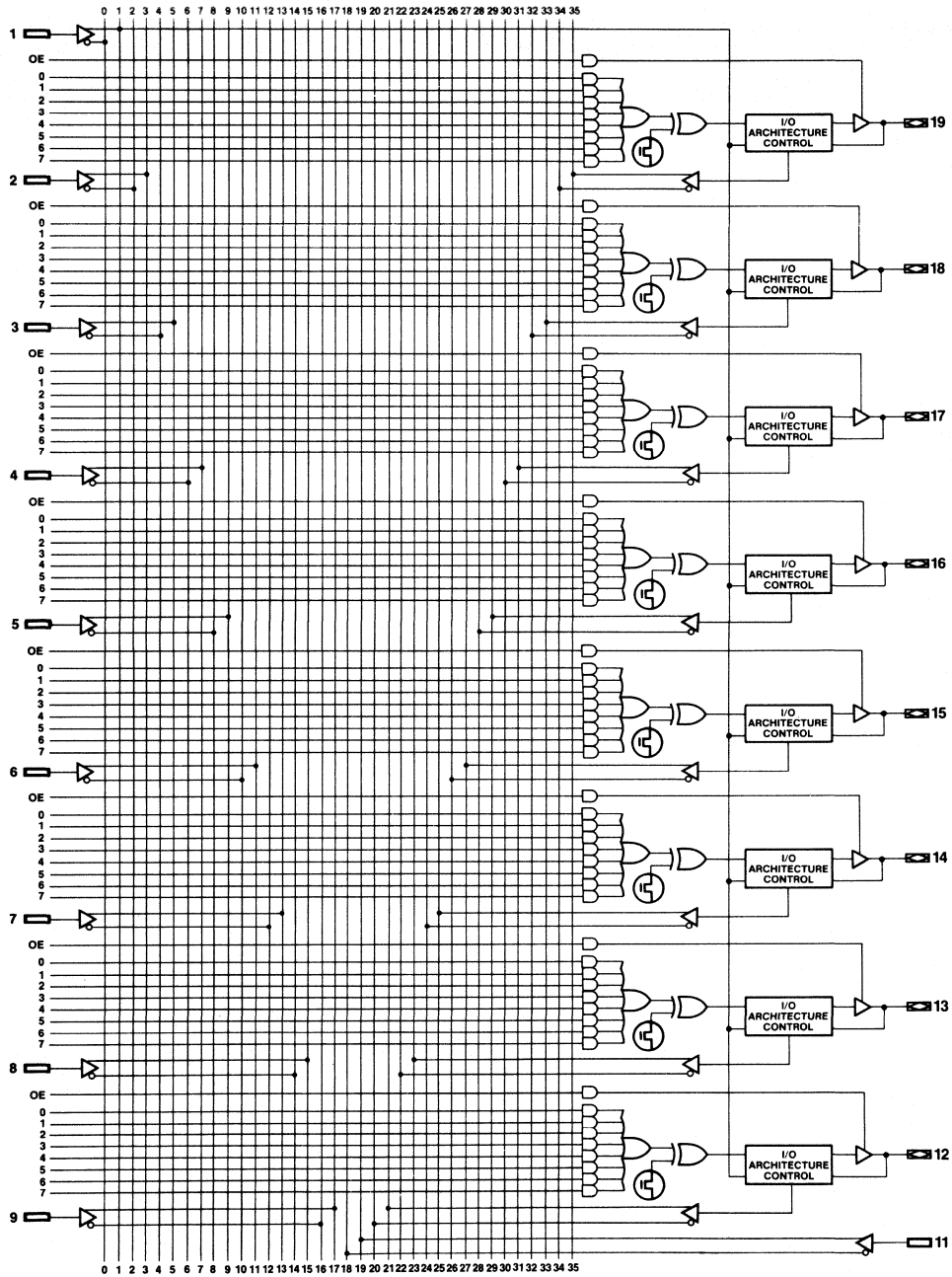
The ALTERA proprietary programmable I/O architecture allows the EP320 user to configure output and feedback paths for combinatorial or registered operation, active high or active low. As a result, the EP320 may be configured as a drop in replacement for PAL devices such as the 16R8 and 16L8.

In addition to architectural flexibility, performance characteristics allow the EP320 to be used in the widest possible range of applications. The CMOS EPROM technology helps make the EP320 a zero power device at standby as well as allowing for an active power consumption of less than 20% of equivalent bipolar devices without sacrifice in speed performance. This technology also facilitates 100% generic testability as well as UV erasability. As a result, designs and design modifications may be quickly implemented upon a given EP320 without the need for post programming testing.



REV. 3.0

FIG. 1 EP320 BLOCK DIAGRAM



ALTERA

Programming the EP320 is made easy with the ALTERA A+PLUS development software (A+PLUS version 4.5 or later release). Using A+PLUS, the user may enter his logic design using schematic capture, netlist entry, Boolean equations and state machine entry. Once the design is entered, A+PLUS performs automatic translation into logical equations, complete Boolean minimization and design fitting directly to an EP320. The device can then be programmed to achieve customized working silicon within minutes at the designer's own desktop.

FUNCTIONAL DESCRIPTION

The EP320 is an Erasable Programmable Logic Device (EPLD) in which CMOS EPROM technology is utilized in order to configure connections in a programmable AND logic array. EPROM connections are also used as a means to control the desired output/feedback options (such as registered or combinatorial, active high or active low).

Externally, the EP320 provides 10 dedicated inputs (one of which may be used as a synchronous clock input) and 8 I/O pins which may be configured for input, output or bi-directional operation.

Figure 1 shows the complete EP320 block diagram, while Figure 2 shows the basic EP320 macrocell. The internal architecture is organized with the familiar sum of products (AND-OR) structure. Inputs to the programmable AND array (seen running vertically in Figure 2) come from two sources: a) the true and complement of the 10 dedicated input pins and; b) the true and complement of 8 feedback signals, each one originating from an I/O Architecture Control Block. The 36 input AND array encompasses a total of 72 product terms distributed equally among the 8 Macrocells. Each product term (seen running horizontally in Figure 1) represents a 36 input AND gate.

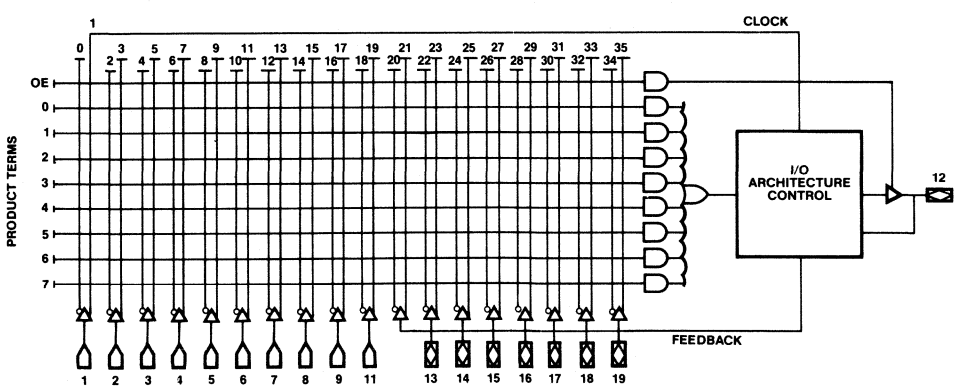
As seen in Figure 1, the outputs of 8 product terms are "ORed" together, then the output of the OR gate is fed as an input to an XOR gate. The purpose for this XOR function is to allow the user to specify the polarity of the output signal by using the "Invert Select" EPROM CELL. (Active high if EPROM cell is programmed, active low if not programmed.) The XOR output then feeds the I/O Architecture Control Block where the output is configured for registered or combinatorial operation. In a registered mode, the output will be registered via a positive edge-triggered D-type flipflop. Under this condition, the feedback signal going back to the array is also registered, coming directly from the output of the D-type flipflop. In a combinatorial mode, the output is non-registered and the feedback signal comes directly from the I/O pin. In the erased state, the EP320 contains the same architectural characteristics as the PAL 16L8.

OUTPUT ENABLE PRODUCT TERM

The Output Enable (OE) product term determines whether an output signal is allowed to propagate to the output pin. If the output of the OE product term is high, output is enabled to the pin. If the output of the OE product term is low, then the output buffer becomes a high impedance node, thus inhibiting the output signal from reaching the output pin. For combinatorial modes, this OE product term can be used to allow for true bi-directional operation.

The EP320 contains 8 separate OE product terms, one per I/O pin. If the user desires all outputs to be enabled or disabled simultaneously, he may do so by using an identically programmed product term at each

FIG. 2 LOGIC ARRAY MACROCELL



Note: ⊠ I/O feedback from a Macrocell

This diagram shows one of the eight Macrocells within the EP320.

of the outputs. If different outputs are to be enabled under different conditions, the user may define a different OE product term for each specific output.

I/O ARCHITECTURE

Figure 3 shows the different output configurations that can be chosen for any of the 8 I/O pins on the EP320. Because of the individuality of each I/O Architecture Control Block, users may choose to have both registered and combinatorial outputs on the same EP320.

In the combinatorial mode, the user may choose either active high or active low output polarity, with an option for pin feedback or no feedback at all.

In the registered mode, the user again has control over output polarity and may choose to use the internal registered feedback path or no feedback at all.

Any I/O pin can be configured as a dedicated input by choosing no output and pin feedback.

In the erased state, the I/O architecture is configured for combinatorial active low output, with pin feedback.

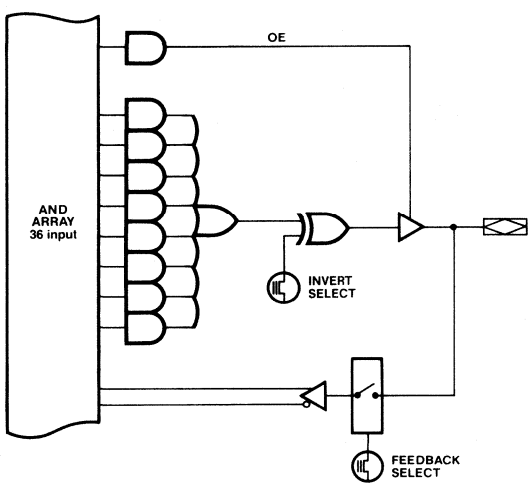
PAL COMPATIBILITY

Figures 4A and 4B show the user how an EP320 can be configured as a drop in replacement for two commonly used members of the 20 pin PAL family, the 16L8 and the 16R8. Notice that when configured in these modes, the EP320 is both a functional as well as a pin to pin replacement for the 16L8 and 16R8.

The tables in Figure 5 give additional information concerning the EP320 as a replacement for the 20 pin PAL family of devices.

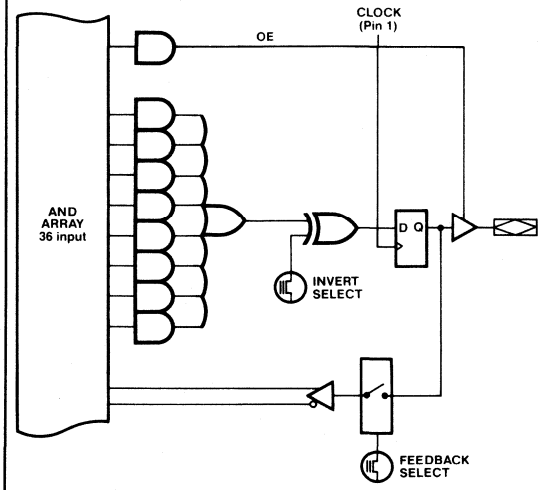
FIG. 3 I/O CONFIGURATIONS

COMBINATORIAL MODE



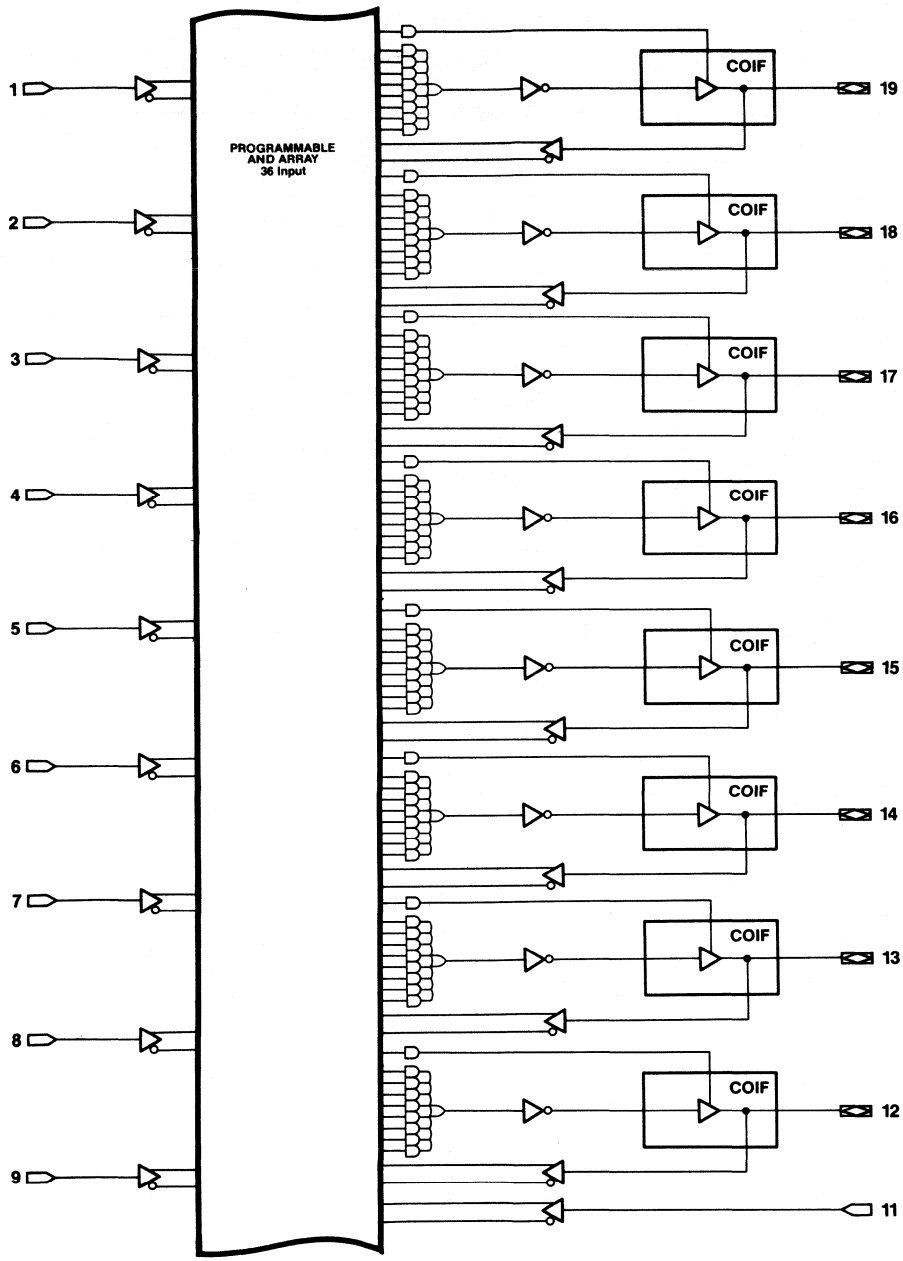
OUTPUT/POLARITY	FEEDBACK
Combinatorial/High	Pin, None
Combinatorial/Low	Pin, None
None	Pin

REGISTERED MODE



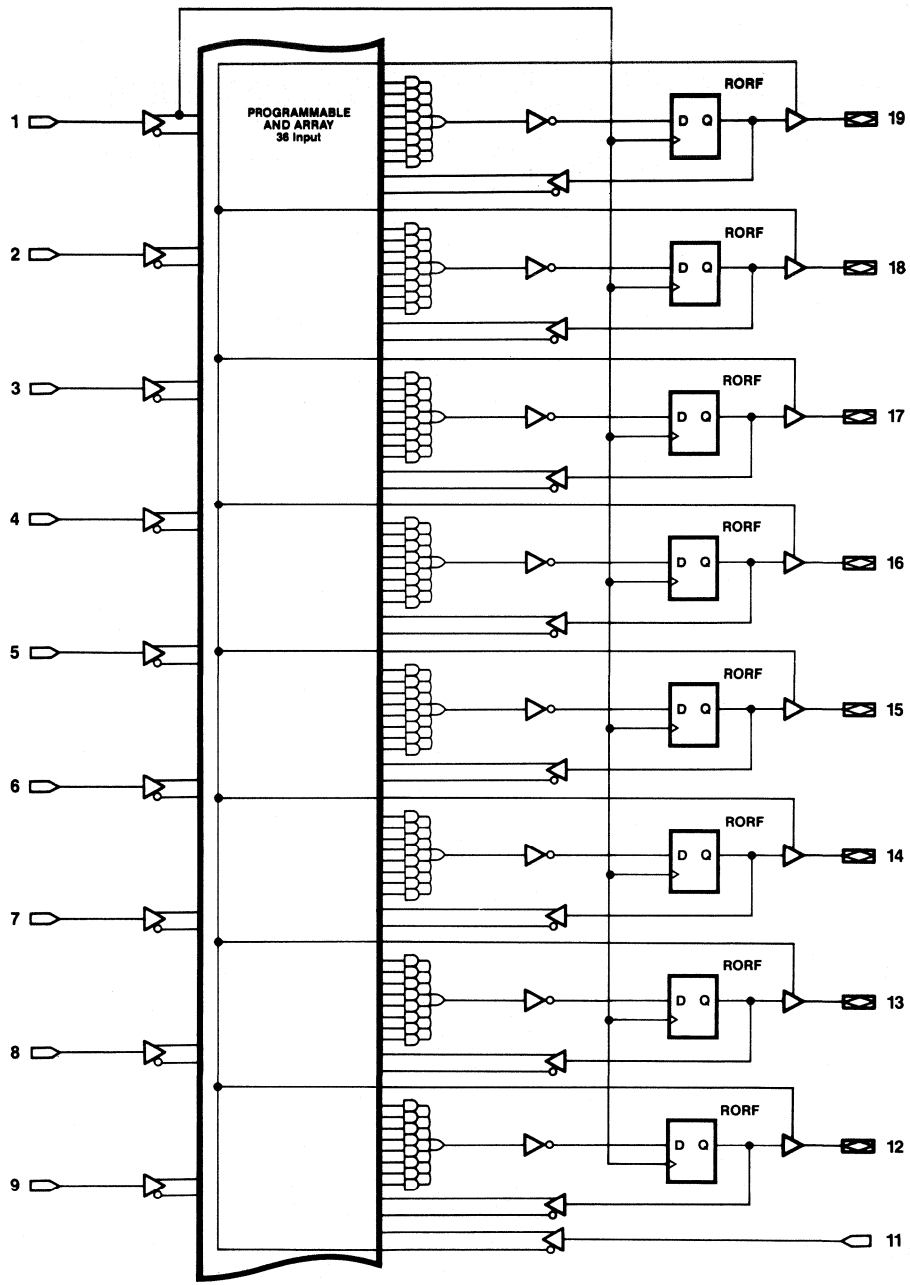
OUTPUT/POLARITY	FEEDBACK
D—Register/High	D—Register, None
D—Register/Low	D—Register, None
None	D—Register

FIG. 4A EP320 USED TO REPLACE PAL 16L8



- "Invert Select" EPROM cell is in the erased state providing active low outputs.
- "Combinatorial Mode" is chosen providing **C**ombinatorial **O**utput with **I**nput (Pin) **F**eedback (COIF).
- 8 product term OR gate compared to 7 product term OR gate on PAL16L8.
- Pin feedback to the array at pins 12, 19 is not available in PAL16L8.

FIG. 4B EP320 USED TO REPLACE PAL 16R8



- "Invert Select" EPROM cell is in the erased state providing active low outputs.
- "Registered Mode" is chosen providing **R**egistered **O**utput with **R**egistered **F**eedback (RORF).
- Complement of pin 11 is used as common OE term for all 8 output pins.

FIG. 5 EP320—PAL CROSS REFERENCE

TABLE 1 EP320 CONFIGURATIONS FOR 20 PIN PAL REPLACEMENT

Pal Part Number	EP320 Pin Number	EP320 Macrocell Number	I/O Configuration Mode	Output/ Polarity	Feedback
10H8	12-19	1-8	Combinatorial	Comb/High	None
10L8	12-19	1-8	Combinatorial	Comb/Low	None
12H6	12 13-18 19	8 2-7 1	Combinatorial Combinatorial Combinatorial	None Comb/High None	Pin None Pin
12L6	12 13-18 19	8 2-7 1	Combinatorial Combinatorial Combinatorial	None Comb/Low None	Pin None Pin
14H4	12-13 14-17 18-19	7-8 3-6 1-2	Combinatorial Combinatorial Combinatorial	None Comb/High None	Pin None Pin
14L4	12-13 14-17 18-19	7-8 3-6 1-2	Combinatorial Combinatorial Combinatorial	None Comb/Low None	Pin None Pin
16C1	12-14 15 16 17-19	6-8 5 4 1-3	Combinatorial Combinatorial Combinatorial Combinatorial	None Comb/Low Comb/High None	Pin None None Pin
16H2	12-14 15-16 17-19	6-8 4-5 1-3	Combinatorial Combinatorial Combinatorial	None Comb/High None	Pin None Pin
16L2	12-14 15-16 17-19	6-8 4-5 1-3	Combinatorial Combinatorial Combinatorial	None Comb/Low None	Pin None Pin
16H8 & 16HD8	12 13-18 19	8 2-7 1	Combinatorial Combinatorial Combinatorial	Comb/High/Z Comb/High/Z Comb/High/Z	None Comb None
16L8 & 16LD8	12 13-18 19	8 2-7 1	Combinatorial Combinatorial Combinatorial	Comb/Low/Z Comb/Low/Z Comb/Low/Z	None Comb None
16R4	12-13 14-17 18-19	7-8 3-6 1-2	Combinatorial Registered Combinatorial	Comb/Low/Z Reg/Low/Z Comb/Low/Z	Comb Reg Comb
16R6	12 13-18 19	8 2-7 1	Combinatorial Registered Combinatorial	Comb/Low/Z Reg/Low/Z Comb/Low/Z	Comb Reg Comb
16R8	12-19	1-8	Registered	Reg/Low/Z	Reg
16P8	12 13-18 19	8 2-7 1	Combinatorial Combinatorial Combinatorial	Comb/Option/Z Comb/Option/Z Comb/Option/Z	None Comb None
16RP4	12-13 14-17 18-19	7-8 3-6 1-2	Combinatorial Registered Combinatorial	Comb/Option/Z Reg/Option/Z Comb/Option/Z	Comb Reg Comb
16RP6	12 13-18 19	8 2-7 1	Combinatorial Registered Combinatorial	Comb/Option/Z Reg/Option/Z Comb/Option/Z	Comb Reg Comb
16RP8	12-19	1-8	Registered	Reg/Option/Z	Reg

TABLE 2 DEVICE SPECIFICATIONS*

		High Speed EPLD	High Speed, Half-Power PAL (Series 20A-2)	
Symbol	Parameter	EP320-2	PAL 16L8A-2	PAL 16R8A-2
t_{pd}	Input to non-registered output	35 ns	35 ns	NA
I_{CC_1}	Supply current standby	150μA	90 mA	90 mA
I_{CC_2}	Supply Current Active f=1MHz	5mA	90 mA	90 mA
t_{CO1}	Clock to output delay	20 ns	NA	25 ns
t_{su}	Input setup time	25 ns	NA	35 ns
f_{max}	Max frequency	40 MHz	NA	16 MHz

* Over commercial temperature range

ABSOLUTE MAXIMUM RATINGS

Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	With respect to GND note (3)	-2.0	7.0	V
V_{PP}	Programming supply voltage		-2.0	13.5	V
V_I	DC INPUT voltage		-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		-80	+80	mA
I_{OUT}	DC OUTPUT current, per pin		-25	+25	mA
P_D	Power dissipation			400	mW
T_{STG}	Storage temperature	No bias	-65	+150	°C
T_{AMB}	Ambient temperature	Under bias	-65	+135	°C
ESD	ElectroStatic Discharge Voltage		±2100		V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage	note (6)	4.75 (4.5)	5.25 (5.5)	V
V_I	INPUT voltage		0	V_{CC}	V
V_O	OUTPUT voltage		0	V_{CC}	V
T_A	Operating temperature	For Commercial	0	70	°C
T_A	Operating temperature	For Industrial	-40	85	°C
T_C	Case temperature	For Military	-55	125	°C
T_R	INPUT rise time			500	ns
T_F	INPUT fall time			500	ns

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = 0°C to 70°C for Commercial)
(V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial)
(V_{CC} = 5V ±10%, T_C = -55°C to 125°C for Military)*
Note (1) and (6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3		0.8	V
V_{OH}	HIGH level TTL output voltage	I_{OH} = -8mA DC	2.4			V
V_{OH}	HIGH level CMOS output voltage	I_{OH} = -4mA DC	3.84			V
V_{OL}	LOW level output voltage	I_{OL} = +8mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	-10		+10	μA
I_{OZ}	3-state output off-state current	V_O = V_{CC} or GND	-10		+10	μA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND No load note (8)		10	150	μA
I_{CC2}	V_{CC} supply current (non-turbo)	V_I = V_{CC} or GND No load, f = 1.0 MHz note (7)		3	5 (15)	mA
I_{CC3}	V_{CC} supply current (turbo)	V_I = V_{CC} or GND No load, f = 1.0 MHz note (7)		18	30 (40)	mA

CAPACITANCE

Note (4)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1.0 MHz		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1.0 MHz		10	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V f = 1.0 MHz		10	pF

AC CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)
(V_{CC} = 5V ± 10%, T_A = –40°C to 85°C for Industrial)
(V_{CC} = 5V ± 10%, T_C = –55°C to 125°C for Military)*

			EP320-1		EP320-2		EP320		NON-TURBO ADDER (note 5)		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t_{PD1}	Input to non-registered output	C_1 = 50pF		29		34		44		15	ns
t_{PD2}	I/O input to non-registered output			30		35		45		15	ns
t_{PZX}	Input or I/O input to output enable			30		35		45		15	ns
t_{PXZ}	Input or I/O input to output disable	C_1 = 5pF note (2)		30		35		45		15	ns
t_{IO}	I/O input buffer delay			1		1		1		0	ns

SYNCHRONOUS CLOCK MODE

			EP320-1		EP320-2		EP320		NON-TURBO ADDER		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
f_{MAX}	Maximum frequency	note (9)	50		40		30.3		0		MHz
t_{SU}	Input or I/O input setup time		20		25		33		15		ns
t_H	Input or I/O input hold time		0		0		0		0		ns
t_{CH}	Clock high time		10		12		16		0		ns
t_{CL}	Clock low time		10		12		16		0		ns
t_{CO1}	Clock to output delay			17		20		25		0	ns
t_{CNT}	Minimum clock period (register output feedback to register input - internal path)	note (7)		35		40		50		0	ns
f_{CNT}	Internal maximum frequency ($1/t_{CNT}$)	note (7)	28.6		25		20		0		MHz

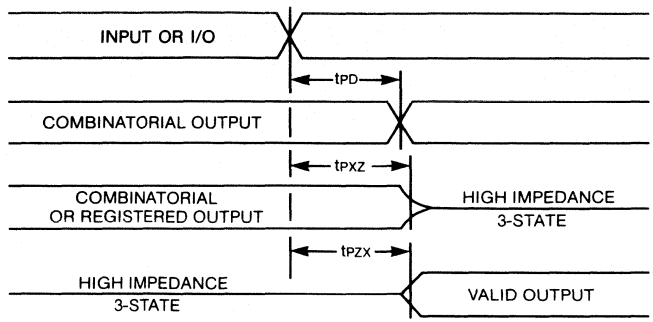
Notes:
1. Typical values are for T_A = 25°C, V_{CC} = 5V
2. Sample tested only for an output change of 500mV.
3. Minimum DC input is –0.3V. During transitions, the inputs may undershoot to –2.0V for periods less than 20ns.
4. Capacitance measured at 25°C. Sample tested only. Pin 11, (high voltage pin during programming), has capacitance of 20 pf max.
5. See TURBO-BIT™, page 2-63.
6. Figures in ( ) pertain to military temperature version.
7. Measured with device programmed as an 8-Bit Counter.
8. EPLD automatically goes into standby mode if logic transitions do not occur when in non-turbo mode (approximately 100 ns after last transition).
9. The f_{MAX} values shown represent the highest frequency for pipelined data.

GRADE	AVAILABILITY	
Commercial (0°C to 70°C)	EP320-1	EP320-2 EP320
Industrial (–40°C to 85°C)		EP320
Military (–55°C to 125°C)		EP320

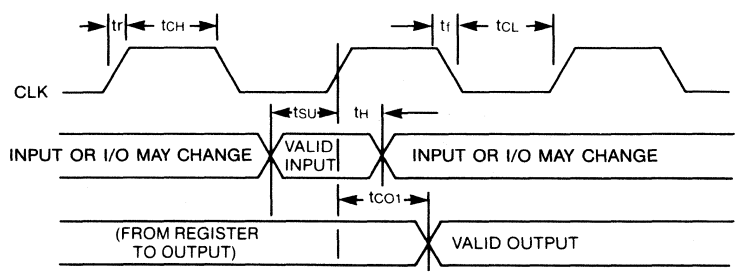
*** Specifications for MIL-STD-883 device may vary from those above. A Military Product Drawing, prepared in accordance with appropriate military specification formats, is available to provide guidance for the preparation of Source Control Drawings (SCD). Please contact Altera Marketing at (408) 984-2800 x 101 to obtain 883 Product drawings.**

FIG. 6 SWITCHING WAVEFORMS

COMBINATORIAL MODE



SYNCHRONOUS CLOCK MODE



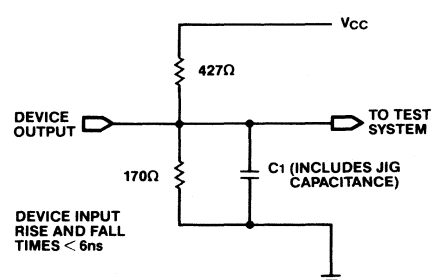
Notes: t_r & $t_f < 6ns$
t_{CL} & t_{CH} measured at 0.3V and 2.7V
all other timing at 1.5V
Input voltage levels at ØV and 3V

FUNCTIONAL TESTING

The EP320 is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

As a result, traditional problems associated with fuse-programmed circuits are eliminated. The erasable nature of the EP320 allows test program patterns to be used and then erased. This facility to use application-independent, general purpose tests is called generic testing and is unique among user-defined LSI logic devices.

FIG. 7 AC TEST CONDITIONS



Power supply transients can affect AC measurements, simultaneous transitions of multiple outputs should be avoided for accurate measurement.
Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

FIG. 8 I_{CC} VS f_{MAX}

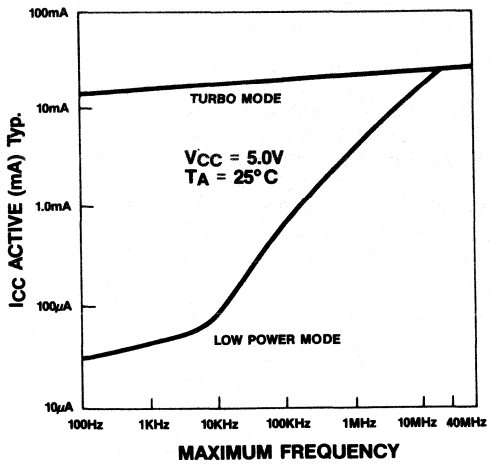
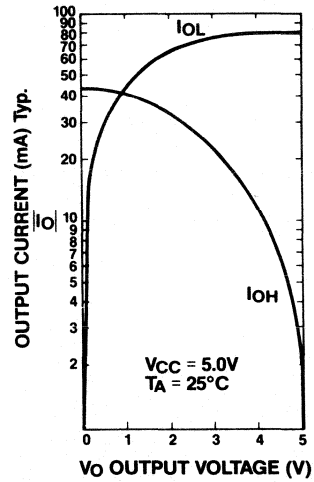


FIG. 9 OUTPUT DRIVE CURRENTS



DESIGN SECURITY

The EP320 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied nor retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

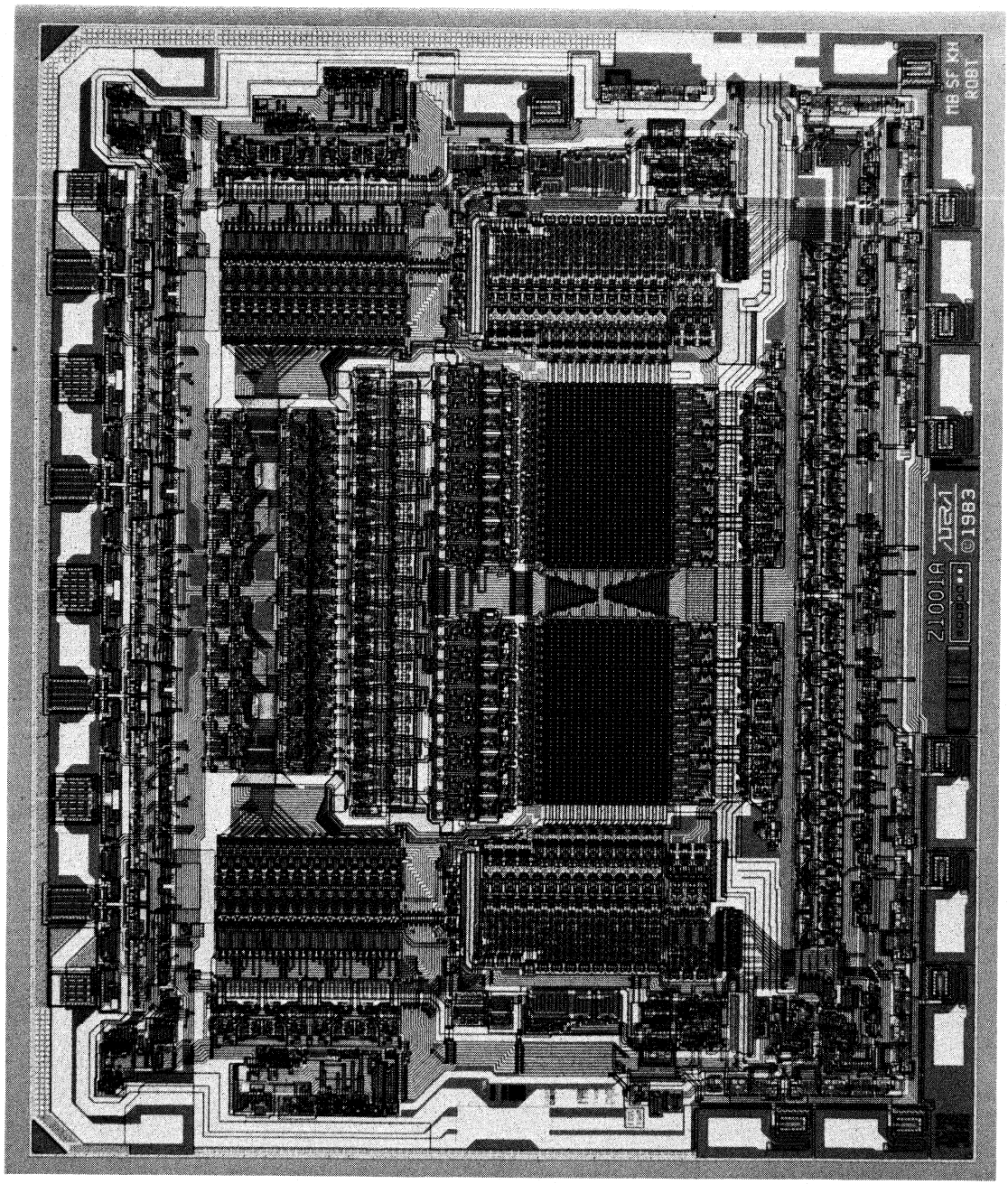
TURBO-BIT

Some EPLDs contain a programmable option to control the automatic power down feature that enables the low standby power mode of the device. This option is controlled by a TURBO-BIT which can be set using A+PLUS. When the TURBO-BIT is programmed (Turbo = ON), the low standby power mode (Icc1) is disabled. This renders the circuit less sensitive to Vcc noise transients which can be created by the power-up/power-down cycle when operating in the low power mode. The typical Icc vs frequency data for both Turbo and Non-Turbo (low power) mode is shown in each EPLD data sheet. All AC values are tested with the TURBO-BIT programmed.

If the design requires low power operation then the TURBO-BIT should be disabled (Turbo = OFF). When operating in this mode, some AC parameters are subject to increase. Values given in the AC specifications section under "Non-Turbo Adder" must be added to the respective AC parameter to determine worst-case timing.

LATCH-UP

The EP320 input, I/O, and clock pins have been carefully designed to resist latch-up which is inherent in CMOS structures. Each of the EP320 pins will not latch-up for input voltages between -1V to V_{CC} + 1V with currents up to 100 mA. During transitions, the inputs may undershoot to -2.0V for periods less than 20 ns. Additionally, the programming pin is designed to resist latch-up to the 13.5 volt maximum device limit.



"The World's first EPLD"

ALTERA

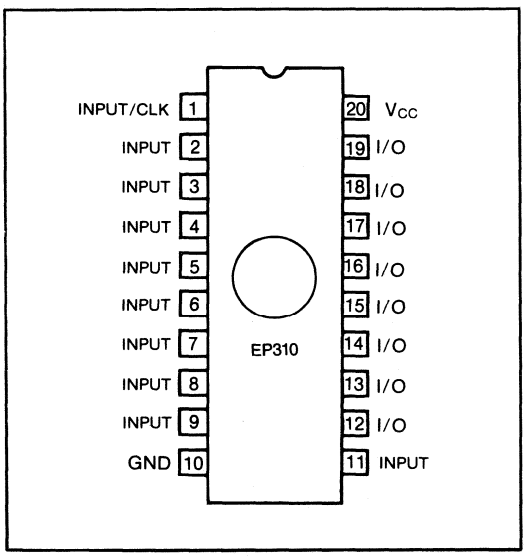
8 MACROCELL EPLD

EP310

FEATURES

- Programmable replacement for conventional fixed logic.
- EPROM technology allows reprogrammability, ensures high programming yield and ease of use.
- Second generation programmable logic architecture allows up to 18 inputs and 8 outputs.
- Each output is *User Programmable* for combinatorial or registered operation, in active high or low mode.
- Each output also has an independently *User Programmable* feedback path.
- 100% generically testable—provides 100% programming yield.
- Programmable "Security Bit" allows total protection of proprietary designs.
- Advanced software support featuring Schematic Capture, Interactive Netlist, Boolean Equation and State Machine design entry.
- Advanced CHMOS II-E circuitry for systems requiring low power, high performance speeds, and immunity to noise.

CONNECTION DIAGRAM

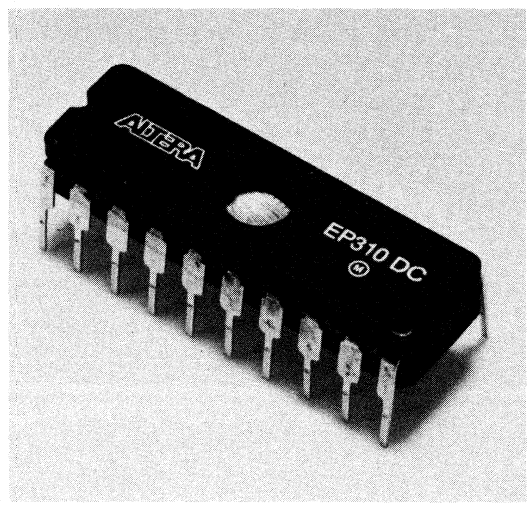


GENERAL DIAGRAM

The ALTERA EP310 combines the power, flexibility, and density advantages of CMOS, EPROM technology with second generation programmable logic array architecture. This combination defines a new capability in electrically programmable logic. The EP310 utilizes the familiar sum-of-products architecture which allows users to program complex custom logic functions quickly and easily. Up to 18 inputs and 8 outputs are provided, with eight product terms and a separate Output Enable term for each output.

A unique feature of the EP310 is the ability to program each output architecture on an individual basis. This gives the user the flexibility to assign either combinatorial or registered output, in either active high or active low mode, to each output pin. In addition, the feedback path can be programmed independently of the output to be either combinatorial, registered, or I/O. Other advantages include: 100% generic testing (all devices are 100% tested at the factory). The device can be erased with ultraviolet light. Design changes are no longer costly, nor is there a need for post programming testing.

Programming the EP310 is accomplished with the use of Altera's A+PLUS development software which supports four different design entry methods. Once the circuit has been entered, the A+PLUS software performs automatic translation into logical equations, boolean minimization, and design fitting directly into an EP310.



REV. 6.0

FUNCTIONAL DESCRIPTION

A block diagram of the EP310, along with logic diagrams of the I/O Architecture Control function and the Logic Array Macrocell are shown in figures 2 and 3. The EP310 is organized in the familiar sum-of-products format with a total of 74 product terms and 36 input lines.

At each intersecting point in the logic array, there exists an EPROM type programmable connection. Initally, all connections are made. This means that both the true and complement of all inputs are connected to each product term. Connections are opened during the programming process. Therefore any product term can be connected to the true or complement of any input. When both the true and complement connection of any input are left intact, a logical false results on the output of the AND gate. If both the true and complement connections of any input are programmed open, then a logical "don't care" results for that input. If all inputs for a product term are programmed open, then a logical true results on the output of the AND gate.

A dramatic improvement in the flexibility of programmable logic is achieved in the ALTERA EP310 through programmable I/O architecture. Each output can be combinatorial (i.e. direct output of the OR gate) or registered (i.e. output through a D type flip-flop). Both types of output can also be inverted. Independent of the output mode, the feedback can be programmed to be combinatorial, registered, I/O (i.e directly from the pin), or none. These features enable the user to optimize the device for precise application requirements.

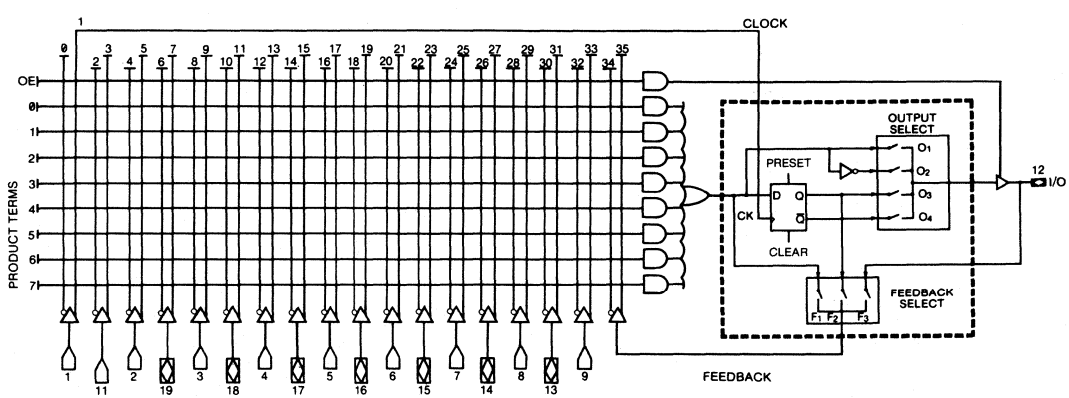
To improve functionality, the ALTERA EP310 has additional Synchronous Preset and Asynchronous Clear product terms. These terms are connected to all D-type Flip-Flops. When the Synchronous Preset product term is asserted (HIGH), the output register will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Clear product term is asserted (HIGH), the output register will immediately be loaded with a LOW (independent of the clock). An Asynchronous Clear overrides a Synchronous Preset requirement. On power-up, the EP310 performs the Clear function automatically.

The EP310 is manufactured using a CMOS EPROM process. This advanced process, along with built in test features, allows 100% pre-test of each programmable connection at the factory.

DESIGN SECURITY

The EP310 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

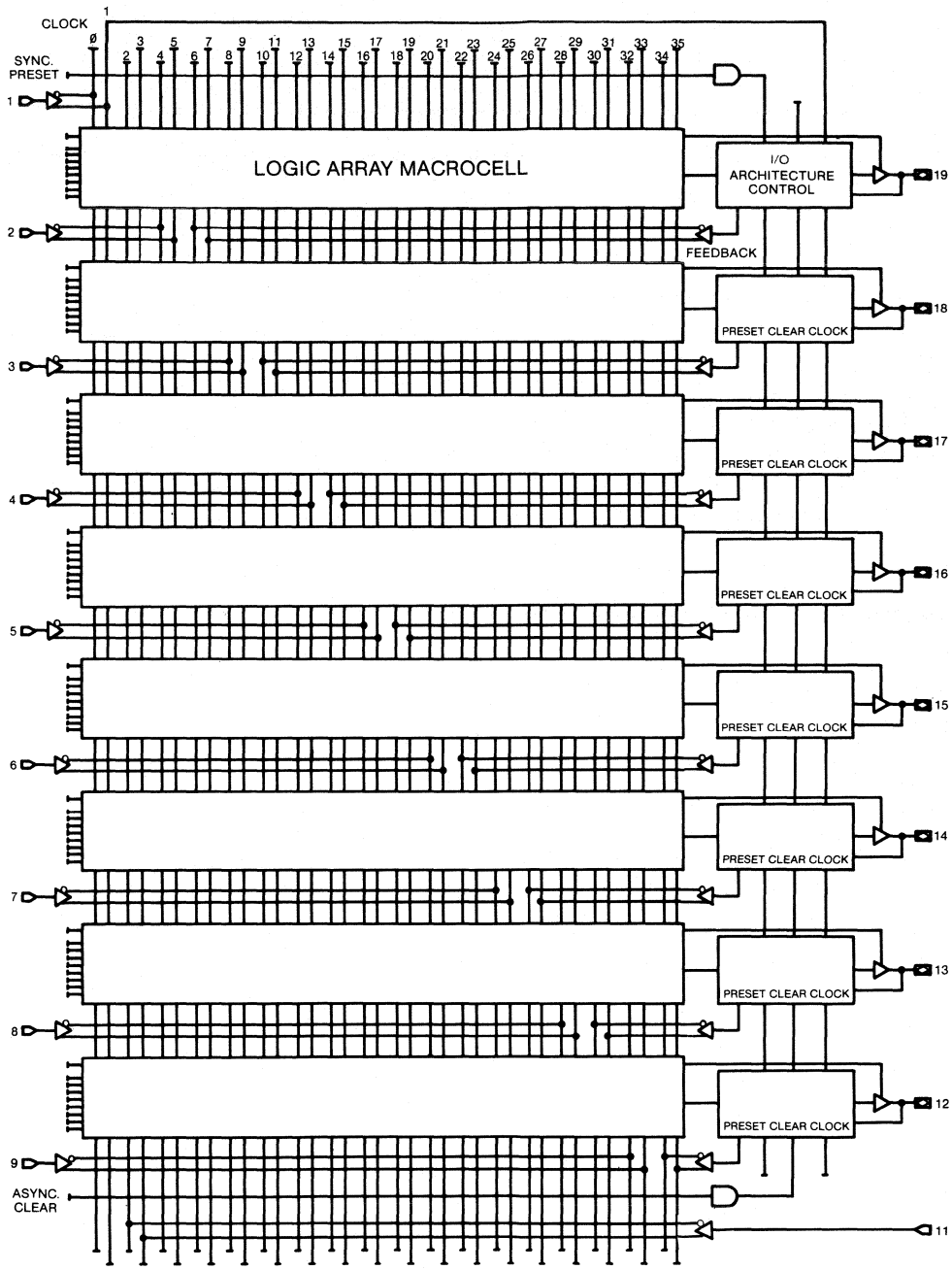
FIG. 2 EP310 MACROCELL



Note: ▯ I/O Pin in which Logic Array input is from feedback path

This diagram shows one of the eight Macrocells within the EP310.

FIG. 3 EP310 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	With respect to GND note (3)	-2.0	7.0	V
V_{PP}	Programming supply voltage		-2.0	13.5	V
V_I	DC INPUT voltage		-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		-80	+80	mA
I_{OUT}	DC OUTPUT current, per pin		-25	+25	mA
P_D	Power dissipation			320	mW
T_{STG}	Storage temperature	No bias	-65	+150	°C
T_{AMB}	Ambient temperature	Under bias	-65	+135	°C
ESD	ElectroStatic Discharge Voltage		±1000		V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage	note (5)	4.75 (4.5)	5.25 (5.5)	V
V_I	INPUT voltage		0	V_{CC}	V
V_O	OUTPUT voltage		0	V_{CC}	V
T_A	Operating temperature	For Commercial	0	70	°C
T_A	Operating temperature	For Industrial	-40	85	°C
T_C	Case temperature	For Military	-55	125	°C
T_R	INPUT rise time			500	ns
T_F	INPUT fall time			500	ns

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = 0°C to 70°C for Commercial)
(V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial)
(V_{CC} = 5V ±10%, T_C = -55°C to 125°C for Military)*
Note (1) and (5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3		0.8	V
V_{OH}	HIGH level TTL output voltage	I_{OH} = -4mA DC	2.4			V
V_{OH}	HIGH level CMOS output voltage	I_{OH} = -2mA DC	3.84			V
V_{OL}	LOW level output voltage	I_{OL} = 4mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	-10		+10	μA
I_{OZ}	3-state output off-state current	V_O = V_{CC} or GND	-10		+10	μA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND No load		15	30 (35)	mA
I_{CC3}	V_{CC} supply current (active)	V_i = V_{CC} or GND No load, f = 1.0 MHz note (6)		16	40	mA

CAPACITANCE

Note (4)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1.0 MHz		12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1.0 MHz		12	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V f = 1.0 MHz		12	pF

AC CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)
(V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial)
(V_{CC} = 5V ± 10%, T_C = -55°C to 125°C for Military)*

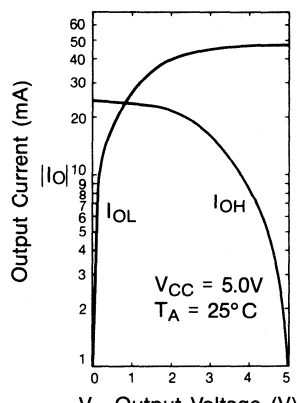
			EP310-2		EP310-3		EP310		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t_{PD1}	Input to non-registered output	C_1 = 30pF		35		40		50	ns
t_{PD2}	I/O input to non-registered output			37		42		52	ns
t_{PZX}	Input to output enable			35		40		50	ns
t_{PXZ}	Input to output disable	C_1 = 5pF note (2)		35		40		50	ns
t_{CLR}	Asynchronous output clear time	C_1 = 30pF		45		50		55	ns
t_{IO}	I/O input buffer delay			2		2		2	ns

SYNCHRONOUS CLOCK MODE

			EP310-2		EP310-3		EP310		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
f_{MAX}	Maximum frequency	note (7)	35.7		33.3		31.3		MHz
t_{SU}	Input setup time		28		30		32		ns
t_H	Input hold time		0		0		0		ns
t_{CH}	Clock high time		14		15		16		ns
t_{CL}	Clock low time		14		15		16		ns
t_{CO1}	Clock to output delay			22		24		28	ns
t_{CNT}	Minimum clock period (register output feedback to register input - internal path)	note (6)		33		37		42	ns
f_{CNT}	Internal maximum frequency ($1/t_{CNT}$)	note (6)	30.3		27.0		23.8		MHz
t_{SET}	Synchronous preset input or I/O input set-up time		28		31		35		ns

Notes:
1. Typical values are for T_A = 25°C, V_{CC} = 5V
2. Sample tested only for an output change of 500mV.
3. Minimum DC input is -0.3V. During transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
4. Capacitance measured at 25°C. Sample tested only. Pin 11, (used for programming), has capacitance of 50pF max.
5. Figures in ( ) pertain to military temperature version.
6. Measured with device programmed as 8-Bit Counter.
7. The f_{MAX} values shown represent the highest frequency for pipelined data.

FIG. 4 OUTPUT DRIVE CURRENTS

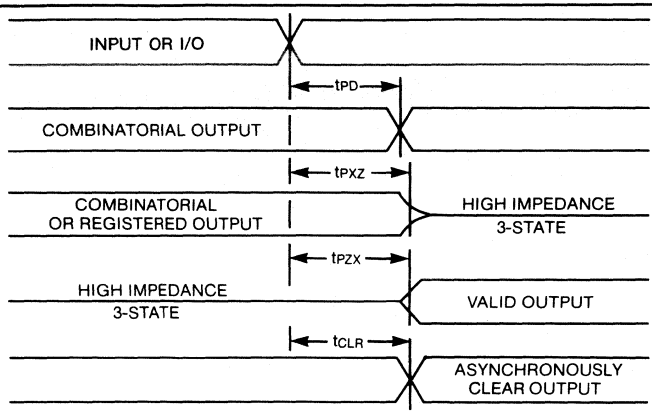


GRADE	AVAILABILITY
Commercial (0°C to 70°C)	EP310-2 EP310-3 EP310
Industrial (-40°C to 85°C)	EP310
Military (-55°C to 125°C)	EP310

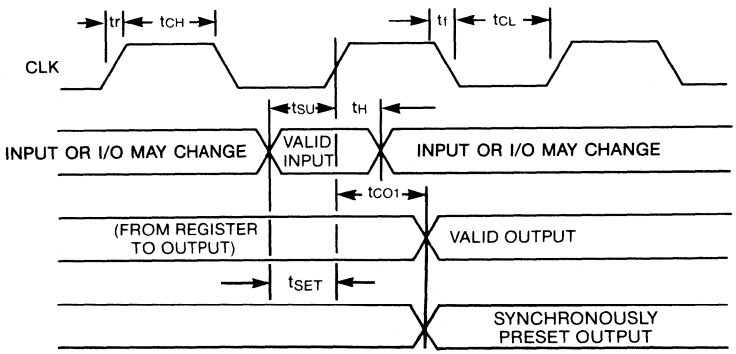
*** Specifications for MIL-STD-883 device may vary from those above. A Military Product Drawing, prepared in accordance with appropriate military specification formats, is available to provide guidance for the preparation of Source Control Drawings (SCD). Please contact Altera Marketing at (408) 984-2800 x 101 to obtain 883 Product drawings.**

FIG. 5 SWITCHING WAVEFORMS

COMBINATORIAL MODE

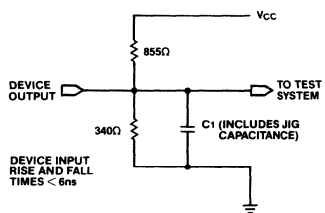


SYNCHRONOUS CLOCK MODE



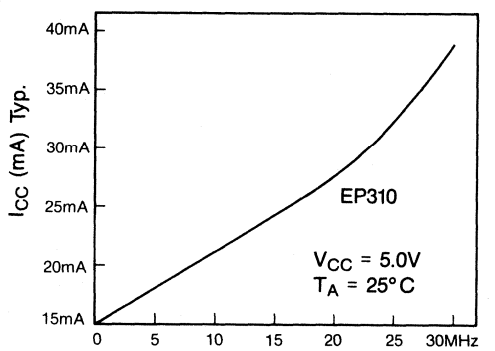
Notes: t_r & t_f < 6ns; t_{CL} & t_{CH} measured at 0.3V and 2.7V; all other timings at 1.5V; Input voltage levels at 0V and 3V

FIG. 6 AC TEST CONDITIONS



Power supply transients can affect AC measurements, simultaneous transitions of multiple outputs should be avoided for accurate measurement. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

FIG. 7 I_{CC} vs. f_{max}

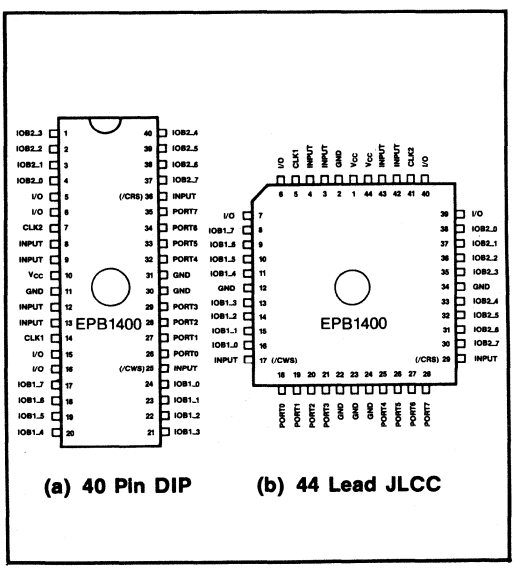


USER-CONFIGURABLE MICROPROCESSOR PERIPHERAL EPB1400

FEATURES

- Bus I/O — Register Intensive (BUSTER) EPLD.
- Erasable, User-Configurable Logic Device for Customized Microprocessor Peripheral Functions.
- Byte-Wide Microprocessor Bus Port with Programmable Control for use with 8, 16 and 32-bit MPUs at up to 25MHz Clock Rate.
- Dual Byte-Wide Input and Output Registers for Fully Buffered Microprocessor Interfacing.
- 20 General Purpose Macrocells Featuring:
  Programmable Flip-Flop Type (D/T/JK/SR)
  Programmable Clocking
  Dual Feedback for Implementing Buried Registers Without Wasting I/O pins.
- 7 Control Macrocells for User-Defined Microprocessor Interface Control.
- Enhanced Drive Capability of 24mA for Direct Connection from Bus Port to External Bus.
- Efficient Design Entry using TTL SSI and MSI Macrofunctions with the Altera Programmable Logic User Software (A+PLUS).
- Packaged in 40 Pin Dual-In-Line (Plastic/ Cerdip) as well as 44 Lead JLCC or PLCC Chip Carriers.

CONNECTION DIAGRAM



(a) 40 Pin DIP **(b) 44 Lead JLCC**

GENERAL DESCRIPTION

The Altera EPB1400 is a user-configurable microprocessor peripheral device. Based on a Bus I/O-Register intensive (BUSTER) architecture, the device is a function-specific Erasable Programmable Logic Device (EPLD) tailored for the design of custom microprocessor peripheral applications.

A typical application environment for the EPB1400 is shown in Figure 1. The unique architecture and high integration density of the EPB1400 yields significant reduction in PC board real estate as well as critical speed enhancement. Integrating control and peripheral functions allows for the replacement of multiple MSI/SSI TTL packages and permits zero wait-state operation with 25 MHz processors. The EPB1400 contains a byte-wide I/O port which may interface to an 8-bit microprocessor directly, or to 16 and 32-bit devices operating in the 8-bit peripheral mode. Multiple EPB1400 devices may be operated in parallel when full 16 or 32-bit I/O is required.

The EPB1400 differs from general purpose programmable logic devices by the addition of specialized interface functions around a state-of-the-art user-configurable logic core. The result is a highly-integrated, user-programmable solution for custom peripheral functions (see Figure 2). Key elements include two byte-wide input functions which may be configured as transparent latches or edge-triggered registers (similar to 74373 or 74377, CMOS or TTL) and two byte-wide output latches (similar to 74373). (Hereafter, the input functions will simply be referred to as input registers.) These byte-wide functions may be used for buffering data from and to the EPB1400 internal bus. Communication to an external bus is provided by an 8-bit bus transceiver (similar to 74245). Enhanced drive capability on the transceiver ports (24mA) allows direct connection to the external bus. Read/Write control for all microprocessor interface functions is provided by two strobe pins and by seven Control Macrocells. These Control Macrocells permit user-defined logic functions to act as control inputs for each of the I/O buffer registers as well as the bus port transceiver. As a result, the EPB1400 may be customized to meet the requirements of any microprocessor bus (e.g., 68020, 80386, 80286, MIL1750A, Z80, etc.)

PRELIMINARY DATA

NOTICE: THIS IS NOT A FINAL SPECIFICATION. SOME PARAMETRIC LIMITS ARE SUBJECT TO CHANGE.

REV. 1.1

In addition to Control Macrocells, the EPB1400 also contains 20 General Purpose Logic Macrocells for implementation of sequential and combinatorial logic functions such as address decoding, interrupt logic and state machines. Each of the General Purpose Macrocells may be configured on an individual basis. Macrocell features such as Dual Feedback, Programmable Flip-flops and Programmable Clocks guarantee maximum pin utility and design flexibility. User-defined logic within a macrocell may be sent directly to an I/O pin or fed back for use by other macrocells. In addition, macrocell feedback may access the EPB1400 internal bus via the I/O buffer registers.

Designing with the EPB1400 is straightforward. Designs may be entered as a mixture of TTL schematics (LogiCaps Schematic Capture and the associated TTL Library, PLSLIB-TTL), state machine files (Altera State Machine Entry, PLSME) and traditional Boolean equations (created with any standard text editor). Once entered, designs are automatically compiled by the Altera Programmable Logic User Software (A+PLUS). The A+PLUS design processor performs complete logic minimization, device fitting and report generation. Within minutes, a standard JEDEC programming file is generated for use in simulation (Altera Functional Simulator, PLFSIM) as well as device programming operations. This integrated design cycle allows designs to be conceived, prototyped, and iterated easily and efficiently.

The EPB1400 utilizes a 1 micron CMOS EPROM technology. User-defined logic functions and architectural configurations are constructed by selectively programming EPROM cells within the device. The EPROM technology guarantees 100% programming yield to the end user due to Generic Testability: all devices are tested 100% at the factory before shipment. Ultraviolet erasable devices enable design iterations to be performed rapidly without additional expense. For volume production needs, plastic One-Time-Programmable (OTP) versions are available.

FUNCTIONAL DESCRIPTION

The EPB1400 has 8 dedicated input pins, 20 I/O pins and 8 bus port pins. The EPB1400 is housed in 40 pin DIP or 44 pin J-lead, surface mount packages.

The EPB1400 detailed block diagram is shown in Figure 3. It contains two key functional blocks, the Microprocessor Interface Block and the Programmable Logic Core Block. Control Macrocells within the Microprocessor Interface Block provide custom control interface to any microprocessor. Of the 8 dedicated input pins, 4 may also be used as strobe inputs to the byte-wide elements in the Microprocessor Interface Block. These byte-wide elements include 2 input buffer registers, 2 output latches and a bus port transceiver. All byte-wide elements communicate via the internal bus.

Figure 1. Typical Microprocessor-Based System

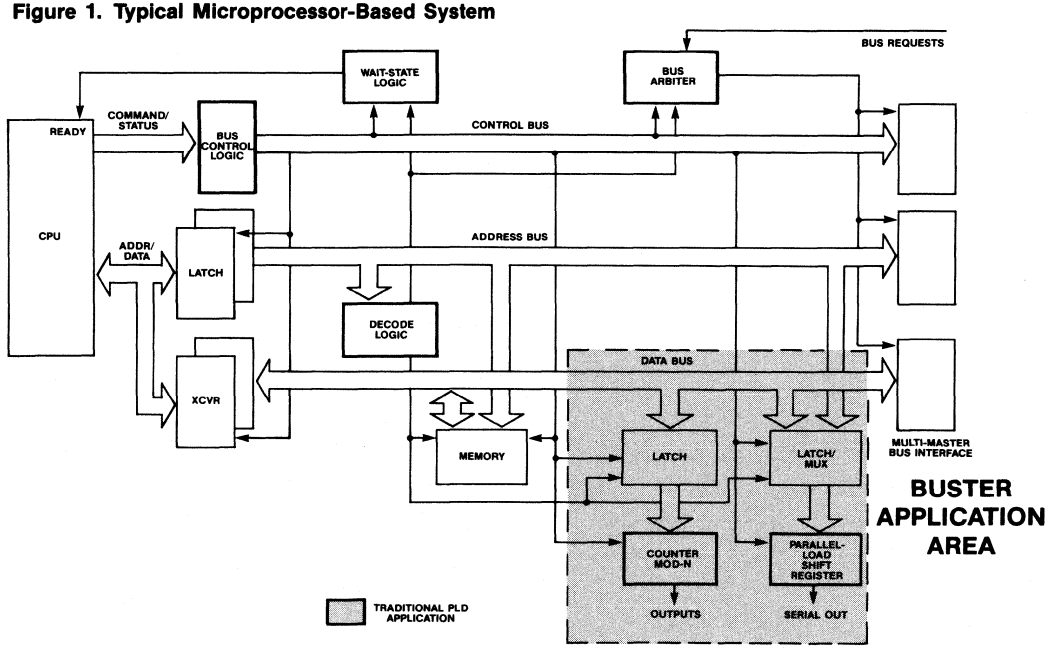
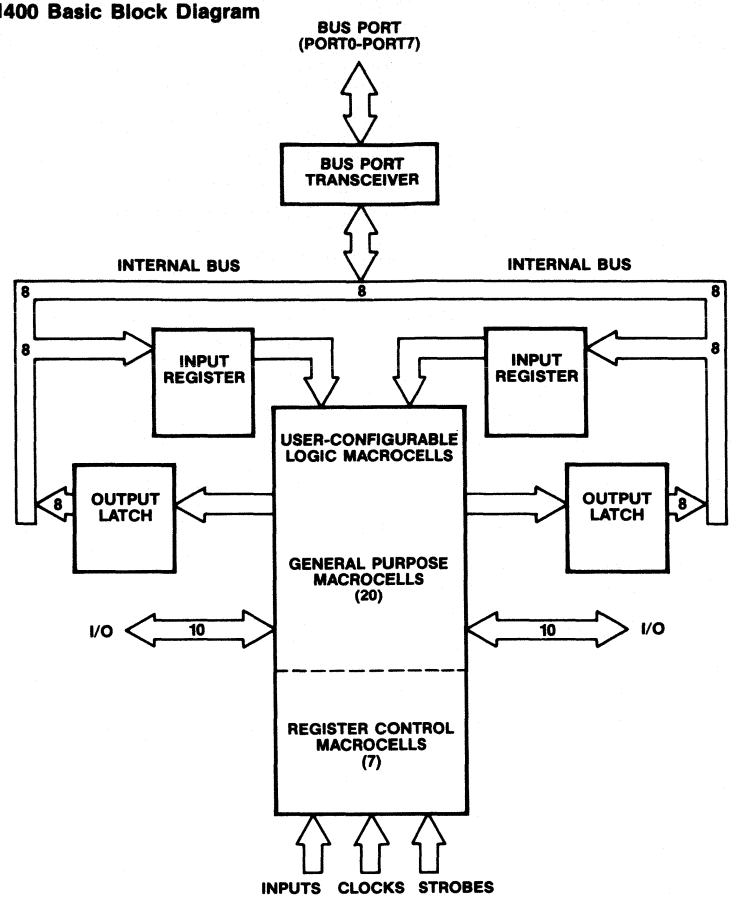


Figure 2. EPB1400 Basic Block Diagram

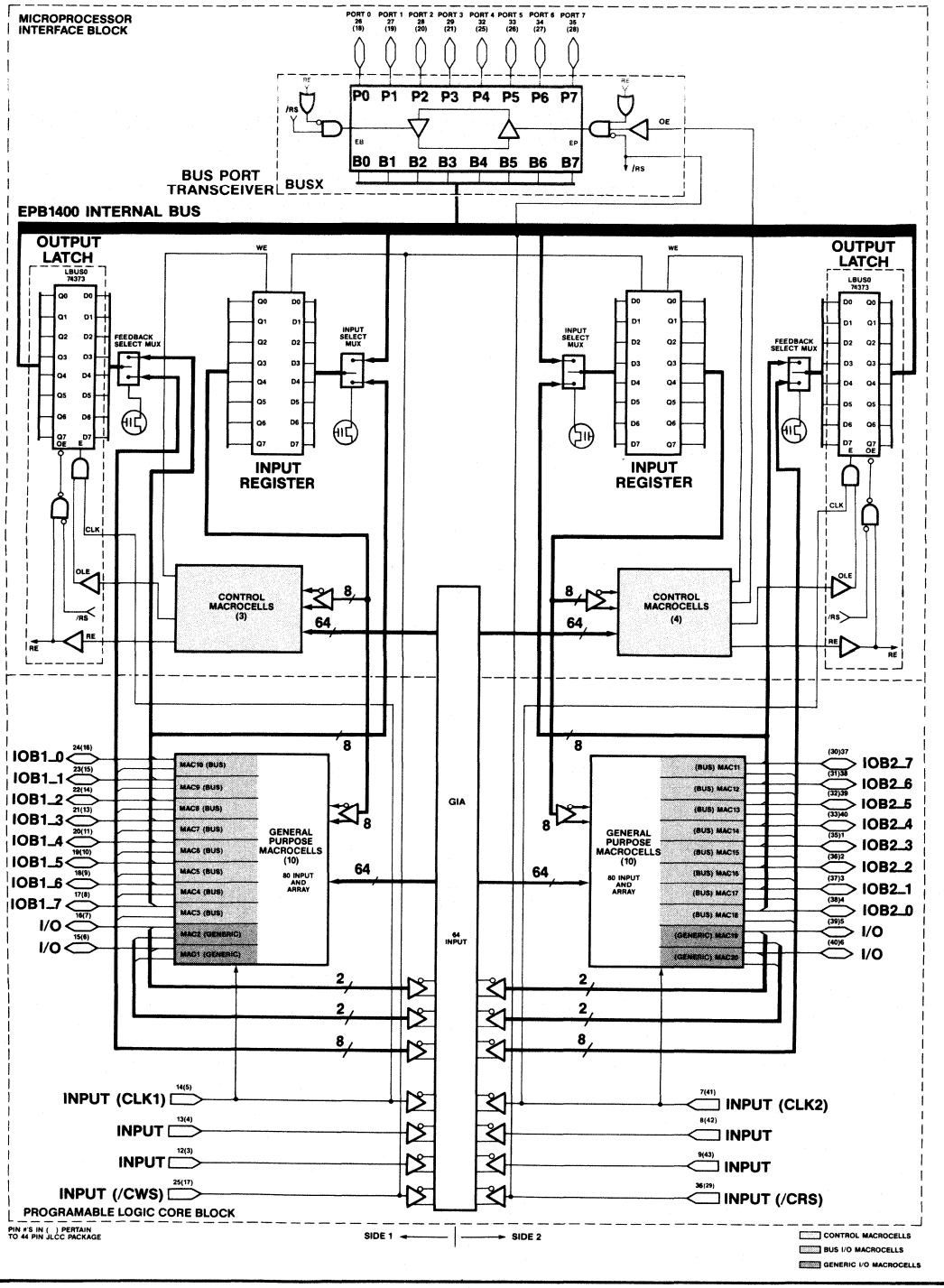


The Programmable Logic Core Block accepts general purpose logic functions related to microprocessor peripheral applications. These may include address decoding, frequency division, parallel/serial data conversions and state machine functions. The Programmable Logic Core contains 20 General Purpose Macrocells. The inputs to these macrocells come from an 80-input logic array consisting of 64 inputs from a Global Interconnect Access (GIA) and 16 feedback signals from input registers within the Microprocessor Interface Block. All macrocells contain programmable options that may be accessed on an individual macrocell basis. These include Dual Feedback, Programmable Flip-flops and Programmable Clocks. All macrocells may be buried internally while associated I/O pins are used as input pins. In addition to feeding the GIA, Macrocell feedback signals may also act as inputs to the input registers and output latches within the Microprocesor Interface Block.

MICROPROCESSOR INTERFACE BLOCK

The architecture of the EPB1400 Microprocessor Interface Block provides fast and efficient access to any microprocessor bus. An 8-bit internal bus is used to connect five byte-wide elements within the Microprocessor Interface Block. These five elements consist of two input buffer registers, two output latches, and a bus port transceiver. Control signals for each byte-wide element are derived within the Control Macrocells on each side. As a result, user-defined logic functions may be used for control of the I/O buffer registers and bus port transceiver.

Figure 3. EPB1400 Detailed Block Diagram



CONTROL MACROCELLS

Figure 4 shows the AND-OR-INVERT structure within each of the seven Control Macrocells. The three Control Macrocells on Side 1 provide control inputs for the buffer registers located on Side 1. The control inputs generated are Write Enable (WE) of the input register, and Output Latch Enable (OLE) and Read Enable (RE) of the output latch. User-defined logic within these Control Macrocells may be a function of any signals within the 80-input Control Array; 16 of these array signals come from the true and complement of the 8 buffered outputs from the input register (Q and /Q), the remaining 64 array signals are contained within the GIA of the EPB1400. Signals within the GIA originate from feedback signals generated by macrocells within the Programmable Logic Core Block as well as signals from input pins to the device.

The four Control Macrocells on Side 2 generate control inputs for the microprocessor interface elements on Side 2. These control inputs are the Write Enable (WE) of the input register, Output Latch Enable (OLE) and Read Enable (RE) of the output latch, and port Output Enable (OE) of the bus port transceiver. User-defined logic within these Control Macrocells may be a function of any signals within the 80-input Control Array, which consists of true and complement feedback signals from the buffered outputs of the input register on the same side (16) as well as signals in the GIA (64).

In situations where minimum skew is desired, the Control Macrocells may be augmented. In this case, fast strobing comes from dedicated input pins of the EPB1400. Pin 25 (/CWS) and Pin 36 (/CRS) provide a fast write strobe and a fast read strobe for the input registers, output latches and bus transceiver port. In addition, Pins 14 and 7 (CLK1 and CLK2) may act as fast clocks for the output latches.

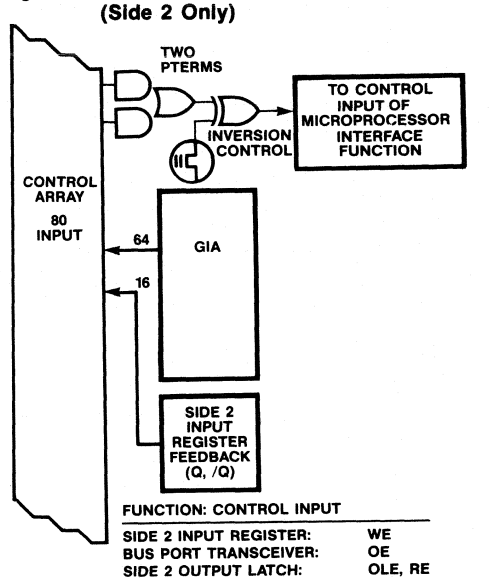
INTERNAL BUS

The 8-bit internal bus forms a highway for communication between the input registers, output latches, and the transceiver port. During normal operation, data passes from the transceiver port to the input register, or from the output latch through the transceiver to the external bus. Data from an output latch may also feed the input register. On-chip bus arbitration circuitry resolves bus contention.

MICROPROCESSOR INTERFACE FUNCTIONS

The Microprocessor Interface Block is equipped with 2 input registers, 2 output registers and the bus port transceiver. Customized peripheral functions are made possible by user-configurable options within these elements. For example, an input register may be configured as an edge-triggered register or as a flow-through latch. Data inputs for the input register may come from a set of input pins or from data off the internal bus. Read, write and output control inputs for each byte-wide element may come from user-defined logic functions in a Control Macrocell as well as pin strobes.

Figure 4. Control Macrocell Architecture (Side 2 Only)

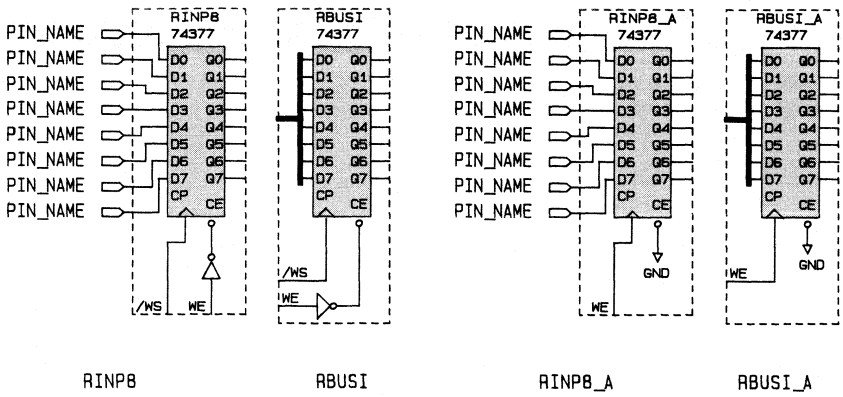


The Microprocessor Interface Functions shown in Figure 5 provide access to the different configurations for the input registers, output latches and bus port transceiver. Definitions for each function are given in Table 1.

During the design entry phase, the Microprocessor Interface Functions are accessed via functions represented by the graphic symbols shown in Figure 5. These 8 functions, along with over 100 standard SSI/MSI functions, are contained in the Altera TTL MacroFunction Library. All functions within this library may be used with the EPB1400.

Complete function tables as well as timing waveforms for each Microprocessor Interface Function are given in Figure 15A through Figure 15F. A brief description with design guidelines follows.

Figure 5. EPB1400 Microprocessor Interface Functions



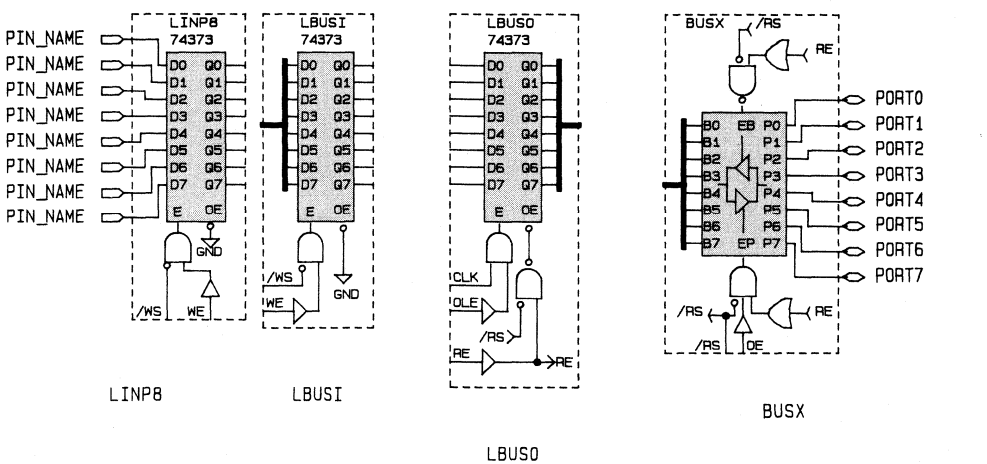


Table 1.

R = REGISTERED (edge-triggered)
L = LATCH (flow-through)

RINP8	8-Bit Input Register(74377) Input from External Pins
RBUSI	8-Bit Input Register(74377) Input from Internal Bus
RINP8_A	8-Bit Input Register(74377) Input from External Pins No Write Strobe (WS)
RBUSI_A	8-Bit Input Register(74377) Input from Internal Bus No Write Strobe (WS)
LINP8	8-Bit Input Latch(74373) Input from External Pins
LBUSI	8-Bit Input Latch(74373) Input from Internal Bus
LBUSO	8-Bit Output Latch(74373) Output to Internal Bus
BUSX	Bus Transceiver(74245) Output to Bus Port Input to Internal Bus

INPUT REGISTERS/LATCHES

RINP8 and RBUSI are edge-triggered input registers similar to the 74377. Fast pin strobing is implemented by connecting the /WS input of the function to the /CWS input pin. The WE control input to the function comes from a user-defined logic function (i.e. a Control Macrocell) and acts as a clock enable input to the registers. I/O pins are the data source for the RINP8 function, while the internal bus is the data source for RBUSI.

Truth tables for the RINP8 and RBUSI functions are shown in Figures 15A and 15B.

RINP8_A and RBUSI_A are also edge-triggered input registers based on the 74377 (similar to RINP8 and RBUSI). No pin strobes are used. Clocking is based solely on the WE control input, which is derived from a user-defined logic function. Triggering occurs on the rising edge of the WE signal. I/O pins are the source for the RINP8_A function, while the internal bus is the source for RBUSI_A.

Truth tables for the RINP8_A and RBUSI_A functions may be derived from Figures 15A and 15B for cases where /WS is not connected. (/WS=NC)

LINP8 and LBUSI are flow-through input latches similar to the 74373. Fast pin strobing is achieved by connecting the /WS control input of the function to the /CWS input pin. If pin strobing is not desired, the /WS control input is connected to an internal ground source. The WE control input of the function comes from a Control Macrocell. These latches pass data when /WS is low and WE is high. I/O pins are the source for the LINP8 function, while the internal bus is the source for LBUSI.

Truth tables for the LINP8 and LBUSI functions are shown in Figures 15C and 15D.

DESIGN GUIDELINES FOR INPUT REGISTERS

The /CWS input pin may always be used as a general purpose input to the GIA. When the /CWS pin is used as a strobe to one input register, then it must also be used as a strobe by the other input register.

When an input register configuration is chosen that uses I/O pins as the data source (RINP8, RINP8_A, or LINP8), the designer may select one of two sets of I/O pins to be used as the D0-D7 inputs for that input register. The two sets of I/O pins are IOB1_0 through IOB1_7 and IOB2_0 through IOB2_7 (see pin connection diagram for pin numbers). If both input registers are configured to have I/O pins as sources, then both sets of I/O pins will be used in that manner. When the designer does not specify which set of I/O pins should be used for a given input register, the A+PLUS software will automatically fit the design, providing complete placement of resources based on circuit interconnectivity. If the input register is placed on Side 1 of the Microprocessor Interface Block, then IOB1_0 through IOB1_7 will directly feed D0-D7 of the input register. For Side 2, IOB2_0 through IOB2_7 will be used.

OUTPUT LATCHES

LBUSO is a flow-through output latch similar to the 74373. The latch enable is based on an AND function of two control inputs, the latch Clock (CLK) and the Output Latch Enable (OLE). Fast pin strobing is implemented by connecting the CLK input of the function to the CLK1 or CLK2 pin. When the CLK input is left unconnected, it is defaulted to an internal VCC source. The OLE input to the function is used to enable the CLK input. OLE is derived from a Control Macrocell. If pin strobing is not used for the CLK input, then the OLE input provides complete latch control.

Output control of LBUSO is an AND function of two signals, the complement of an active-low Read Strobe (complement of /RS), and Read Enable (RE). The /RS is active when pin strobing is used on the bus port transceiver (BUSX). In this case, the /RS control input of the BUSX function is connected to the /CRS pin. Under these conditions, the RE input to the AND gate of LBUSO acts as an enable signal for the /RS signal. The RE input is derived from a Control Macrocell. When the bus port transceiver does not use pin strobing, the /RS signal defaults to an internal ground connection. Under these conditions, the RE control input to LBUSO has complete control over the output enable function for the output latch.

A truth table of the LBUSO function is shown in Figure 15E.

DESIGN GUIDELINES FOR OUTPUT LATCHES

When the CLK control input of one output latch is used for pin strobing from the CLK1 pin and the remaining output latch uses pin strobing, then the CLK control input of the remaining output latch must be connected to the CLK2 pin. Whenever pin strobes are not used, the CLK control input of the output latch defaults to an internal VCC connection. The CLK1 and CLK2 input pins may always be used as general purpose inputs to the GIA. In addition, the CLK1 and CLK2 pins may be used as clock signals for the General Purpose Macrocells on Side 1 and Side 2, respectively.

The /RS control input is common among both output latches and the bus port transceiver. When pin strobing is used, the /RS control input must be connected to the /CRS pin. Like other pin strobes, the /CRS input pin may always be used as a general purpose input to the GIA. OLE and RE come from Control Macrocells and are independent of other control functions.

The RE input to LBUSO may affect the RE input to BUSX (bus transceiver). For possible implications, please see Design Guidelines for Bus Port Transceiver.

The data source of an output latch is determined by the connections to the D0-D7 inputs of the output latch. As shown in Figure 3, the D0-D7 connections come from one of two possible sources: 1) internal (buried) feedback from a group of General Purpose Macrocells (Bus I/O type) within the Programmable Logic Core Block, or 2) external (from the I/O pin) feedback from the same set of macrocells. In addition to choosing internal or external macrocell feedback, the designer may specify which group of Bus I/O Macrocells should be fed to an output latch. If the group of Bus I/O Macrocells is on Side 1 of the EPB1400, then the D0 to D7 inputs to the output latch will come from feedback signals derived in Macrocell 10 to Macrocell 3, respectively. Similarly, Macrocell 18 through Macrocell 11 are used when Side 2 is specified. These macrocells are called Bus I/O Macrocells because their feedback signals are routed on buses to byte-wide elements within the Microprocessor Interface Block. If no specifications are made, A+PLUS software invokes its automatic fitting algorithm to fit the design.

BUS PORT TRANSCEIVER

BUSX is similar to the 74245 bi-directional bus transceiver. Directional control over the transceiver is achieved by logic functions that are based on control inputs to the BUSX function. A three-input AND gate enables data from the internal bus to pass to the external port. Inputs to this AND gate consist of the following control signals: 1) an active-low Read Strobe (/RS); 2) an Output Enable signal (OE); and 3) a Read Enable input (RE). The /RS control input to the BUSX function is connected to the /CRS pin for pin strobing. Otherwise, the unconnected /RS control input defaults to an internal ground connection. The OE control input is derived within a Control Macrocell. The RE signal is the logical OR of the RE inputs related to the LBUSO output latch functions used in the design. When /RS,OE and RE take on the logic levels Low, High and High respectively (a read operation), data will be passed from the internal bus to the external microprocessor bus.

A two-input NAND gate controls data transmission from the external microprocessor bus to the internal bus of the EPB1400. The control inputs to this NAND gate are /RS and RE. When /RS is at a high logic level or RE is at a low logic level (no read operation), then data from the external bus port will be transferred to the internal bus.

A truth table for the BUSX function is shown in Figure 15F.

DESIGN GUIDELINES FOR BUS PORT TRANSCEIVER

In order to guarantee proper Read operation and avoid bus contention, the RE input to the bus port transceiver cannot be connected directly to the BUSX function. Instead, the RE input to BUSX is the logical OR function of the RE inputs on LBUSO functions. This avoids simultaneous transfer of data to the internal bus by both the bus transceiver and either output latch.

PROGRAMMABLE LOGIC CORE

Figure 3 details the Programmable Logic Core Block. General Purpose Macrocells allow the implementation of user-defined mixes of combinatorial and sequential logic functions such as address decoding, interrupt logic and state machines.

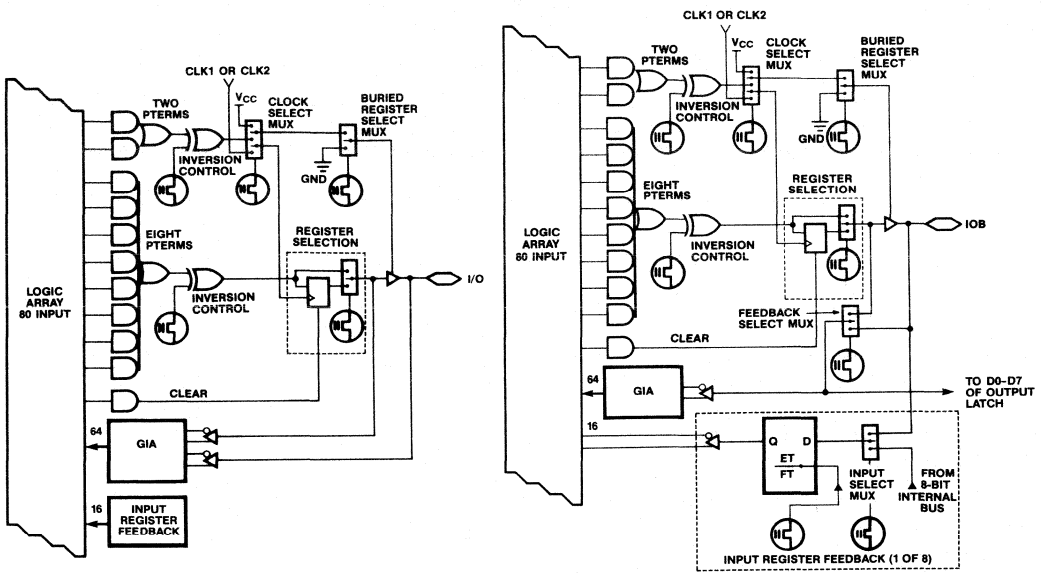
GENERAL PURPOSE MACROCELLS

A total of 20 General Purpose Macrocells, 10 located on each side, are contained within the Programmable Logic Core Block. All General Purpose Macrocells are fed by an 80-input logic array; 64 of the array signals come from the GIA while the remaining 16 come from an input register within the Microprocessor Interface Block. The 64 array signals from the GIA are comprised of the true and complement form of all dedicated input pins (16), all General Purpose Macrocell internal feedback signals (40) and all external Generic I/O Macrocell feedback signals (8). As a result, each product term is equivalent to an 80-input AND gate.

Within each group of General Purpose Macrocells, there are two types of macrocells, Generic I/O and Bus I/O. Each side has 2 Generic I/O Macrocells and 8 Bus I/O Macrocells. Figure 6A shows the composition of the Generic I/O Macrocell. Figure 6B shows the Bus I/O Macrocell.

Common features among the Generic I/O and Bus I/O Macrocells include programmable flip-flop

Figure 6A, 6B. General Purpose Macrocell Architecture



(A) Generic I/O Type **(B) Bus I/O Type**

options, programmable clock/OE options and programmable register clear functions. Both macrocell types may be configured as D,T,JK or SR flipflops. Flip-flop selection may be bypassed for purely combinatorial outputs. The programmable clock feature allows selection of either a dedicated clock pin (CLK1 or CLK2) or a user-defined logic function to clock the macrocell flip-flop. The logic resources allocated for this user-definable clock signal accommodate up to 2 product terms with optional inversion control. This function is shared by the output enable (OE) function of the macrocell. As a result, if either CLK1 or CLK2 is used to clock the flip-flop, then the 2 product term logic network is used for the programmable OE function. Conversely, when the 2 product term network is used for clocking of the flip-flop, then OE must be attached to either VCC or GND, corresponding to a permanently enabled output or a buried register. One independent product term is used to perform an asynchronous clear function on the flip-flop. When the Clear product term goes to a high level, the Q output of the macrocell goes to a low level, independent of the flip-flop clock.

Both types of macrocells also contain a dual feedback feature. Dual Feedback allows a macrocell to be used internally for buried functions while the associated macrocell pin is used as an input pin. The distinction between Generic I/O and Bus I/O Macrocells is related to the destination of these dual feedback signals.

The 4 Generic I/O Macrocells (2 on each side) contain internal and external feedback to the GIA. They are not used as direct data inputs to byte-wide resources in the Microprocessor Interface Block. However, the 16 Bus I/O Macrocells (8 on each side) contain feedback that can act as inputs to the GIA and byte-wide inputs to the Microprocessor Interface Block. The diagram in Figure 6B shows that the designer has the option to choose between internal feedback or external feedback from Bus I/O Macrocells via a Feedback Select Mux. Once chosen, the feedback signals may act as inputs to the GIA as well as the D0 to D7 inputs for the output latch on the same side as the Bus I/O Macrocells. In addition, the external feedbacks (pins IOB1_0 through IOB1_7 or pins IOB2_0 through IOB2_7) may act as the D0 through D7 inputs to the input register on the same side.

ADDITIONAL BURIED REGISTERS

Applications which do not employ both input registers or both output latches in the Microprocessor Interface Block may use the unused elements as buried registers. The 8-bit internal data bus transports data from the output latches to input registers. The input registers pass bytes of data which are accessed in true and complement form by Control Macrocells and General Purpose

Macrocells. Applications which do not use any of the input or output latches can tap up to 32 additional buried register bits. Control over these additional buried registers is maintained through the use of independently programmable Control Macrocells.

Pipelining operations are also made possible. Single stage pipelining uses either a vacant input register or vacant output latch as an 8-bit buried register. For double stage pipelining, data may be clocked in both the output latch and input register, each of which may be converted to an 8-bit buried latch or register.

The bus port transceiver can be transformed into 8 additional input pins. In normal use, the port transceiver passes data from an external port to the internal bus where it may feed the input registers in the Microprocessor Interface Block. Therefore, data can be taken from the 8 port pins (PORT0-PORT7), pass through a flow-through latch, and ultimately access logic arrays used by Control Macrocells and General Purpose Macrocells.

EPB1400 DESIGN SUPPORT — A+PLUS

Complete CAE/CAD support for EPB1400 designs is provided through Altera Programmable Logic User Software (A+PLUS). This provides a PC-based development environment which permits a variety of design entry options, performs automatic logic minimization and design fitting, and produces an object code device programming file. In addition, functional verification of designs is possible through the use of simulation tools.

EPB1400 designs may be entered using schematic capture, state machine entry or traditional Boolean equation entry formats. A mixture of these input mechanisms is accepted by the A+PLUS design processor.

The Altera LogiCaps Schematic Capture package provides an efficient and simple to use entry method for design of the EPB1400. Macrofunction libraries access over 100 popular TTL SSI/MSI functions as well as the 8 microprocessor interface functions shown in Figure 5. LogiCaps features 10 levels of zoom, split-screen capability, real-time orthogonal rubberbanding, user-definable macro definition with optional tail-end recursion, bus and multi-page support.

Designs may also be entered using a high level state machine input language. This format uses IF_THEN_ELSE constructs as well as a mixture of truth tables and Boolean expressions.

Design processing is automatic. The A+PLUS design processor performs macrofunction reduction and decomposition (MacroMunching), complete logic minimization, and design fitting. The design processor consists of translator, minimizer, and fitter modules. The Translator performs design rule checking for logical consistency and completeness. The Minimizer uses artificial intelligence techniques that allow for complete logic reduction, resulting in full optimization of EPLD resources. The Fitter matches the design requirements with the EPLD resources, then intelligently assigns pin numbers which satisfy all internal connections. The end result is an industry standard JEDEC file which can act as an input to simulation software for complete functional verification of the design. Once simulation is complete, the JEDEC file is used to program the EPB1400 with programming software and hardware available to support all Altera development system options.

CALCULATING DELAY PATHS

A timing model for the Programmable Logic Core Block is shown in Figure 7 and associated waveforms are shown in Figure 8. Timing of external paths is given in Figure 9. Additional parametric relationships are shown in Figures 10A and 10B as well as in Figures 11A and 11B. Delay paths related to the Microprocessor Interface Functions are shown in Figure 15A through Figure 15F.

To calculate path delays within the Programmable Logic Core Block, begin at the start of the path in Figure 7 and follow the path to its completion, summing the delay of each block traversed by the path. For example, Figure 10A calculates the delay from input to combinatorial output (T_{PD}). T_{PD} is obtained by starting at the input pin, traversing the logic array, and exiting from the output pin. From this path, T_{PD} becomes the sum of the input delay (t_{IN}), the logic array delay (t_{LAD}) and the output delay (t_{OD}). Parameters related to registers are not taken into account for a combinatorial function. Figure 10B shows the calculation of T_{CNT}.

Delay paths that traverse the Microprocessor Interface Block must use the delay components noted in Figure 15A through Figure 15F. The sample calculation in Figure 11A shows the delay necessary to read data from an output latch into the bus port after the /CRS signal (T_{RSD}).

Delay paths that involve both the Microprocessor Interface Block and the Programmable Logic Core Block may also be calculated. The calculation in Figure 11B determines the delay necessary to write data to the input register (based on the /CWS strobe), then have that data appear on a combinatorial output.

FUNCTIONAL TESTING

Functional and parametric operation of the EPB1400 is guaranteed through complete testing of each programmable EPROM bit and all internal logic elements, thus ensuring 100% programming yield. The erasable nature of the EPB1400 allows test program patterns to be used and then erased.

Figure 7. Programmable Logic Core Block Delay Paths

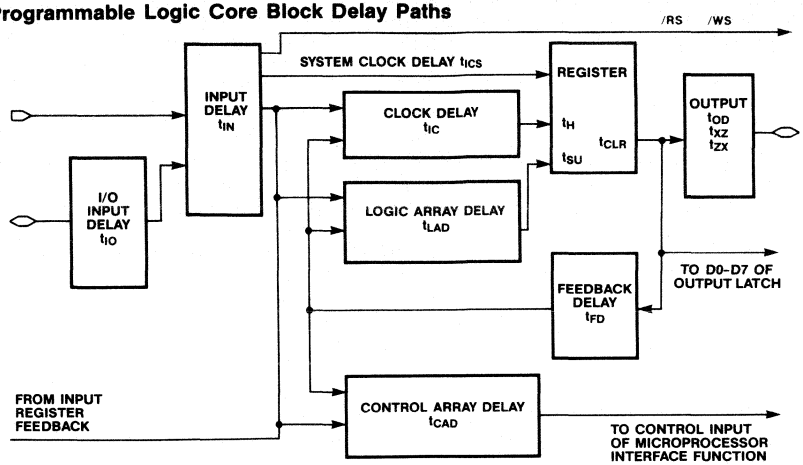
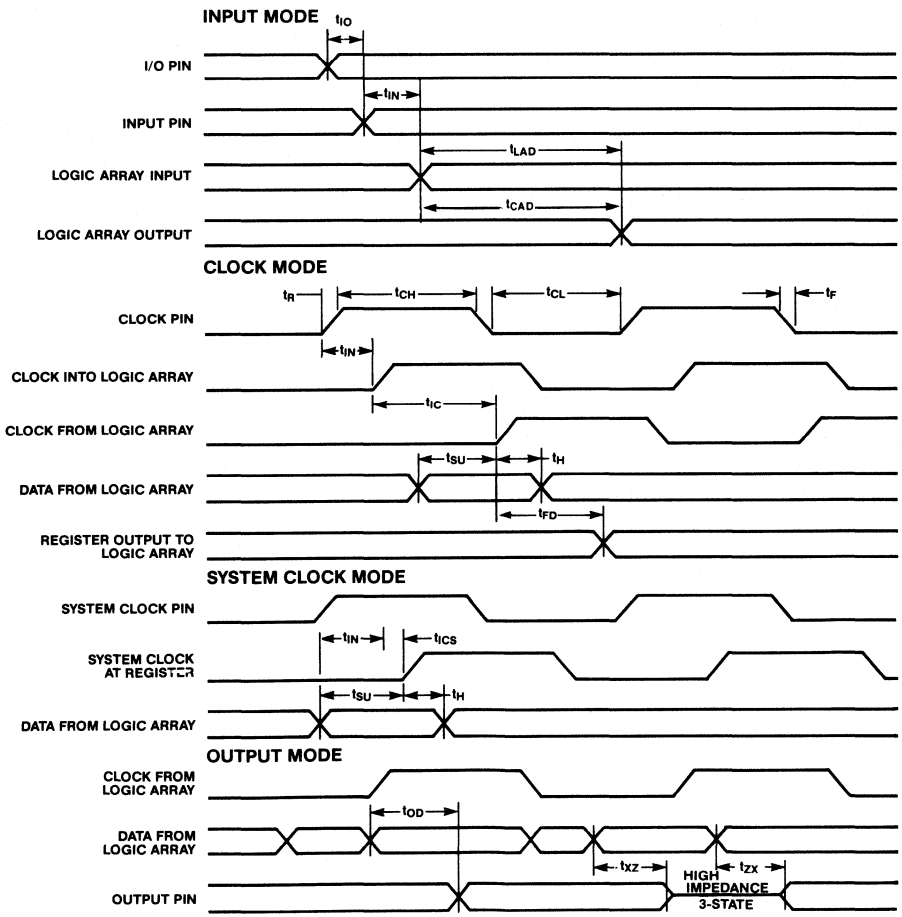


Figure 8. Switching Waveforms



ABSOLUTE MAXIMUM RATINGS

Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	With respect to GND note (3)	-2.0	7.0	V
V_{PP}	Programming supply voltage		-2.0	13.5	V
V_I	DC INPUT voltage		-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		-550	+550	mA
I_{OUT}	DC OUTPUT current, per I/O pin		-25	+25	mA
I_{OUT}	DC OUTPUT current, per Bus Port pin		-50	+50	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	-65	+150	°C
T_{AMB}	Ambient temperature	Under bias	-65	+135	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage		4.75	5.25	V
V_I	INPUT voltage		0	V_{CC}	V
V_O	OUTPUT voltage		0	V_{CC}	V
T_A	Operating temperature		0	70	°C
T_R	INPUT rise time	note (6)		250	ns
T_F	INPUT fall time	note (6)		250	ns

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)
Note (1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3		0.8	V
V_{OH}	HIGH level TTL output voltage	I_{OH} = -4mA DC	2.4			V
V_{OH}	HIGH level CMOS output voltage	I_{OH} = -2mA DC	3.84			V
V_{OH}	HIGH level TTL output voltage (Bus Port)	I_{OH} = -4mA DC	2.4			V
V_{OL}	LOW level output voltage	I_{OL} = 4mA DC			0.50	V
V_{OL}	LOW level output voltage (Bus Port)	I_{OL} = 24mA DC			0.50	V
I_I	Input leakage current	V_I = V_{CC} or GND	-10		+10	μA
I_{OZ}	3-state output off-state current	V_O = V_{CC} or GND	-10		+10	μA
I_{CC3}	V_{CC} supply current	V_I = V_{CC} or GND No load, f = 1.0MHz note (5)		70		mA

CAPACITANCE

Note (4)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{PORT}	Bus Port Pin Capacitance	V_{OUT} = 0V f = 1.0 MHz		15	pF
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1.0 MHz		20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1.0 MHz		25	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V f = 1.0 MHz		20	pF

AC CHARACTERISTICS

EPB1400-2, EPB1400

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)

			EPB1400-2			EPB1400			
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{MAX}	Maximum clock frequency	note (7)		35			29		MHz
t_{IN}	Input pad and buffer delay			8			10		ns
t_{IO}	I/O input pad and buffer delay			3			5		ns
t_{LAD}	Logic Array delay			18			24		ns
t_{CAD}	Control Array delay			18			24		ns
t_{OD}	Output buffer and pad delay	C_1 = 35pF (Fig 12)		9			11		ns
t_{ZX}	Output buffer enable			9			11		ns
t_{XZ}	Output buffer disable	C_1 = 5pF note (2)		9			11		ns
t_{SU}	Register set-up time			10			12		ns
t_H	Register hold time			10			12		ns
t_{CH}	Clock high time			14			17		ns
t_{CL}	Clock low time			14			17		ns
t_{IC}	Clock delay			18			24		ns
t_{ICS}	System clock delay			3			4		ns
t_{FD}	Feedback delay			7			9		ns
t_{CLR}	Register clear time			23			29		ns
t_{CNT}	Minimum clock period (register output feedback to register input-internal data)			35			45		ns
f_{CNT}	Internal maximum frequency ($1/t_{CNT}$)	note (5)		29			22		MHz

Notes:
1. Typical values are for T_A = 25°C, V_{CC} = 5V
2. Sample tested only for an output change of 500mV.
3. Minimum DC input is -0.3V. During transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
4. Capacitance measured at 25°C. Sample tested only. Clock pin capacitance for dedicated clock inputs only. Pin 12, (high voltage pin during programming), has capacitance of 120pF max.
5. Measured with device programmed as a 20 bit counter.
6. Clock t_R, t_F = 25ns.
7. The f_{MAX} values shown represent the highest frequency for pipelined data.

These preliminary specifications are provided for evaluation purposes. Conservative values are shown prior to full device characterization. Please request a copy of the current EPB1400 Electrical Specification for complete information.
A Military Product Drawing will be prepared, in accordance with appropriate military specification formats, to provide guidance for the preparation of source control drawings (SCD).

Figure 9. External Timing Paths

			EPB1400-2			EPB1400			
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
t_{WSQ}	/CWS to input register output valid			14			19		ns
t_{WSD}	Bus port or IOB to /CWS setup			7			11		ns
t_{WSH}	Bus port or IOB to /CWS hold			9			12		ns
t_{RSD}	/CRS to bus port valid			29			39		ns
t_{SOV}	CLK1 or CLK2 to bus port valid			34			46		ns
t_{PD1}	Input to non-registered output			35			45		ns
t_{CO1}	CLK1 or CLK2 to output			20			25		ns

Switching Waveforms

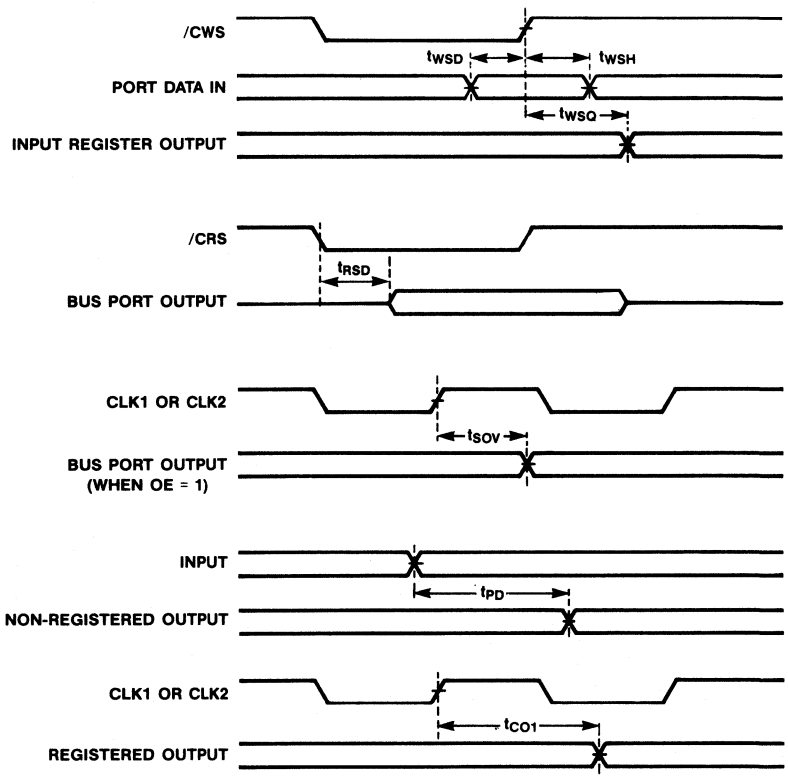
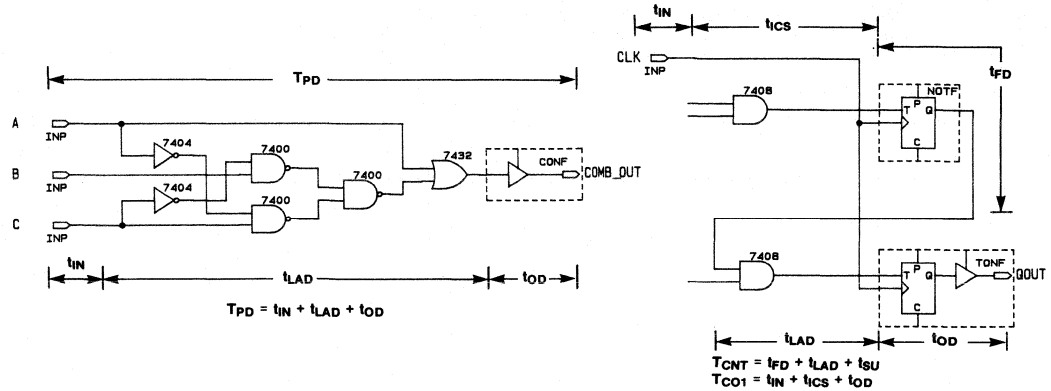


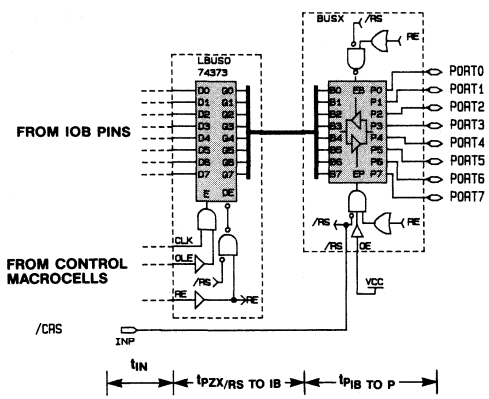
Figure 10A, 10B. Parametric Relationships within Programmable Logic Core Block



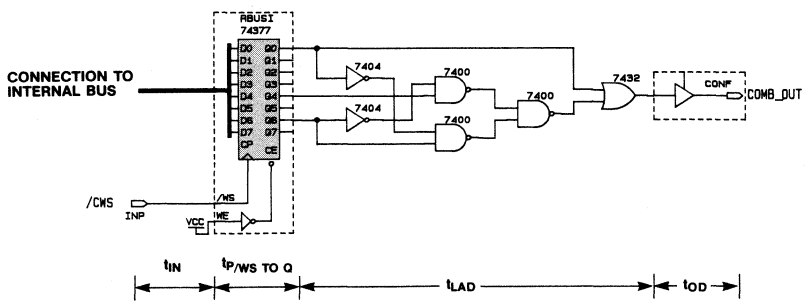
(A) T_{PD}, Delay from Input to Combinatorial Output

(B) T_{CNT}, Minimum Clock Period
(Delay from register output feedback to register input, on the internal path)
T_{CO1}, Delay from Clock to Output

Figure 11A, 11B. Parametric Relationships within the Microprocessor Interface Block



(A) T_{RSD}, Read Strobe Delay
(Delay to read the data from an Output Latch into the Bus Port, after the /CRS pin is asserted.)



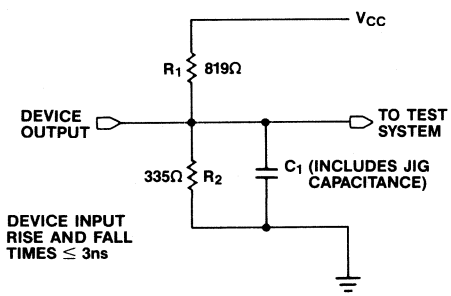
(B) Input Register Read to Combinatorial Output
(Delay from the time the /CWS pin is asserted to the time a combinatorial output is valid.)

This ability to perform application-independent, general purpose tests is called Generic Testing and is unique to erasable, user-configurable logic devices. Non-windowed, OTP versions of the EPB1400 combine erasable testing cycles at the wafer level with special on-chip test circuitry, used after packaging, to achieve 100% programming yield.

DESIGN SECURITY

The EPB1400 contains a programmable design security feature that controls access to data programmed into the device. If this programmable feature is used, the custom pattern in the device is free from interrogation or reverse engineering since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset by erasing the device.

Figure 12. AC Test Conditions

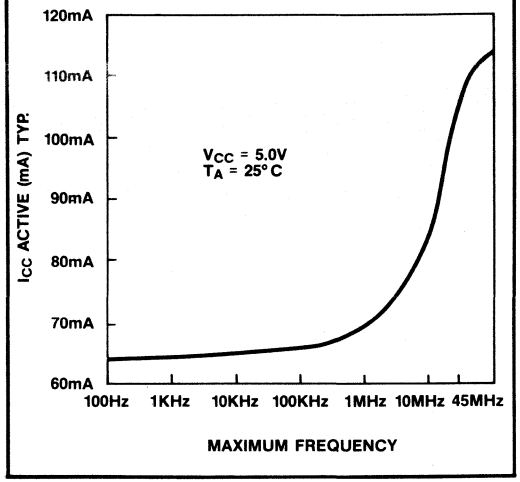


Power supply transients can affect AC measurements, simultaneous transitions of multiple outputs should be avoided for accurate measurement. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity. Bus port measurements should use R_1 and R_2 values of 159Ω and 118Ω, respectively, with C_1 = 100pF.

PROGRAM ERASURE

Erasure of the programmed connections in the EPB1400 begins to occur on exposure to light wavelengths shorter than 4000 Angstroms. Note that sunlight and certain fluorescent lighting can erase a programmed EPB1400 since they have wavelengths in the range of 3000 to 4000 Angstroms. Constant exposure to room level fluorescent lighting could erase an EPB1400 in approximately 3 years. Direct sunlight could cause erasure in approximately 1 week. If the EPB1400 is to be exposed to these conditions for extended periods of time, an opaque label should be placed over the window.

Figure 13. I_{CC} vs F_{MAX}



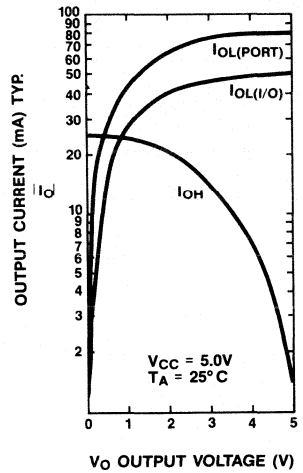
The recommended erase procedure for the EPB1400 is exposure to shortwave ultraviolet light with a wavelength of 2537 Angstroms. The integrated dose for erasure should be a minimum of 30Wsec/cm². The erasure time with this dosage is approximately 45 minutes using an ultraviolet lamp with a 12000 μW/cm² power rating. The EPB1400 should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated exposure dose for an EPB1400 without damage is 7000 Wsec/cm². This is approximately one week at 12000 μW/cm². Exposure of the EPB1400 to high intensity UV light for long periods of time may cause permanent damage.

The EPB1400 may be erased and re-programmed as many times as needed using the recommended erasure exposure levels.

LATCH-UP & ESD PROTECTION

EPB1400 input, I/O, and clock pins have been designed to resist electro-static discharge (ESD) and latch-up damage. Each of the EPB1400 pins will withstand voltage energy levels exceeding those specified by MIL STD 883C. EPB1400 pins will not latch-up for input voltages between -1V to VCC+1V with currents up to 100mA. During transitions the inputs may undershoot to -2.0V for periods less than 20ns. Additionally, the programming pin is designed to resist latch-up to the 13.5V maximum device limit.

Figure 14. Output Drive Currents



DESIGN RECOMMENDATIONS

Operation of devices described herein with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The EPB1400 contains circuitry to protect inputs against high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

For proper operation, it is recommended that an opaque labels be placed over the device window. Input and output pins must be constrained to the range GND $<$ (V_{IN} or V_{OUT}) $<$ V_{CC}. Unused inputs must always be tied to an appropriate logic level (e.g. either V_{CC} or GND). Each set of V_{CC} and GND pins must be shorted together directly at the device. Power supply decoupling capacitors of at least .2μF must be connected between V_{CC} and GND. For the most effective decoupling, connect one capacitor between each set of V_{CC} and GND pins, directly at the device.

PACKAGE OUTLINES

Package outlines for the EPB1400 40 Pin DIP and 44 Pin JLCC/PLCC packages are shown in the Altera 1987 Databook, pages 4-17 and 4-18.

DEVELOPMENT SYSTEM REQUIREMENTS

The recommended development environment for design of the EPB1400 is the Altera PLCAD-SUPREME EPLD Development System. PLCAD-SUPREME includes all modules within the A+PLUS Software (version 5.0 or later release required for support of the EPB1400) as well as the LogiCaps Schematic Capture Package, macrofunction libraries, a functional simulator, a master programming module and selected adapters. In addition, a PLED1400 or PLEJ1400 device adapter must be purchased to support the EPB1400 device. For more information concerning development systems, please contact Altera Corporation.

The recommended system requirements for the Altera PLCAD-SUPREME Development System are as follows:

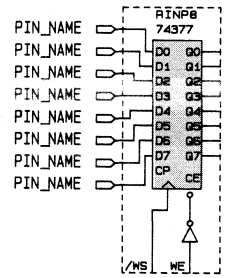
- IBM XT, AT or compatible computers
- CGA, EGA (with extended memory), or Hercules Graphics Adapter
- 640 KBytes RAM
- 10 Mbyte hard disk drive and 5¼ inch floppy drive
- DOS version 3.1 or later release
- 3-Button serial Mouse, Logitech LogiMouse (model C7) or Mouse Systems PC Mouse. Connects to serial port of computer.

Figure 15A. RINP8—Input Register, Data from IOB Pins

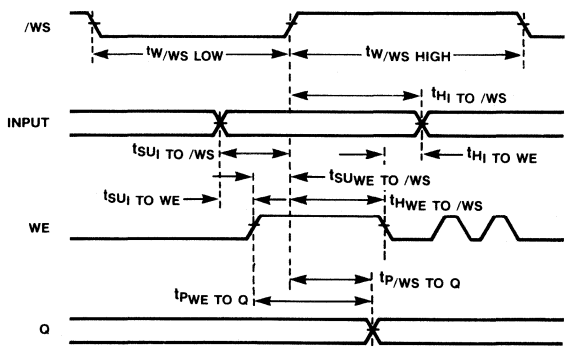
Truth Table

/WS	WE	I	Q	Q^+
↑	H	L	X	L
↑	H	H	X	H
H	X	X	L	L
H	X	X	H	H
L	X	X	L	L
L	X	X	H	H
NC [1]	↑	L	X	L
NC [1]	↑	H	X	H

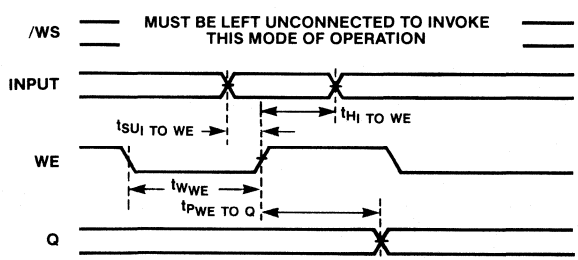
[1] When /WS is not connected (/WS = NC), operation reflects the RINP8_A function.



SYMBOL	PARAMETER	EPB1400-2 MIN	EPB1400-2 TYP	EPB1400-2 MAX	EPB1400 MIN	EPB1400 TYP	EPB1400 MAX	UNIT
t_W	Pulse duration of /WS high		30			40		ns
	Pulse duration of /WS low		15			20		ns
	Pulse duration of WE		20			25		ns
t_{SU}	Input to /WS		3			5		ns
	WE to /WS		10			15		ns
	Input to WE		2			4		ns
t_H	Input to /WS		5			8		ns
	WE to /WS		2			4		ns
	Input to WE		5			8		ns
t_P	/WS to Q		6			9		ns
	WE to Q		8			12		ns



MODE 1: WRITE STROBE USED



MODE 2: WRITE STROBE NOT USED

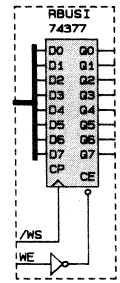
Figure 15B. RBUSI—Input Register, Data from Internal Bus

Truth Table

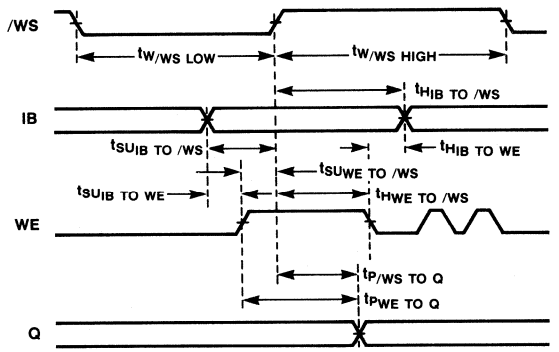
/WS	WE	IB	Q	Q^+
↑	H	L	X	L
↑	H	H	X	H
H	X	X	L	L
H	X	X	H	H
L	X	X	L	L
L	X	X	H	H
NC [1]	↑	L	X	L
NC [1]	↑	H	X	H

IB—INTERNAL BUS

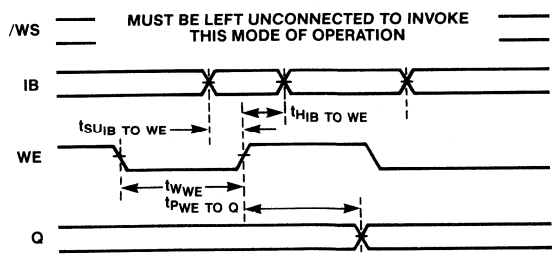
[1] When /WS is not connected (/WS = NC), operation reflects the RBUSI_A function.



SYMBOL	PARAMETER	EPB1400-2 MIN	EPB1400-2 TYP	EPB1400-2 MAX	EPB1400 MIN	EPB1400 TYP	EPB1400 MAX	UNIT
t_W	Pulse duration of /WS high		30			40		ns
	Pulse duration of /WS low		15			20		ns
	Pulse duration of WE		20			25		ns
t_{SU}	Internal Bus to /WS		3			5		ns
	WE to /WS		10			15		ns
	Internal Bus to WE		2			4		ns
t_H	Internal Bus to /WS		5			8		ns
	WE to /WS		2			4		ns
	Internal Bus to WE		5			8		ns
t_P	/WS to Q		6			9		ns
	WE to Q		8			12		ns



MODE 1: WRITE STROBE USED

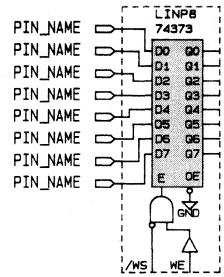


MODE 2: WRITE STROBE NOT USED

Figure 15C. LINP8—Input Latch, Data from IOB Pins

Truth Table

/WS	WE	I	Q	Q^+
L	H	L	X	L
L	H	H	X	H
H	X	X	L	L
H	X	X	H	H
X	L	X	L	L
X	L	X	H	H



		EPB1400-2			EPB1400			
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
t_W	Pulse duration of /WS high		30			40		ns
	Pulse duration of /WS low		15			20		ns
	Pulse duration of WE		20			25		ns
t_{SU}	Input to /WS		3			5		ns
	WE to /WS		10			15		ns
	Input to WE		2			4		ns
t_H	Input to /WS		5			8		ns
	WE to /WS		2			4		ns
	Input to WE		5			8		ns
t_P	/WS to Q		6			9		ns
	WE to Q		8			12		ns
	Input to Q		6			9		ns

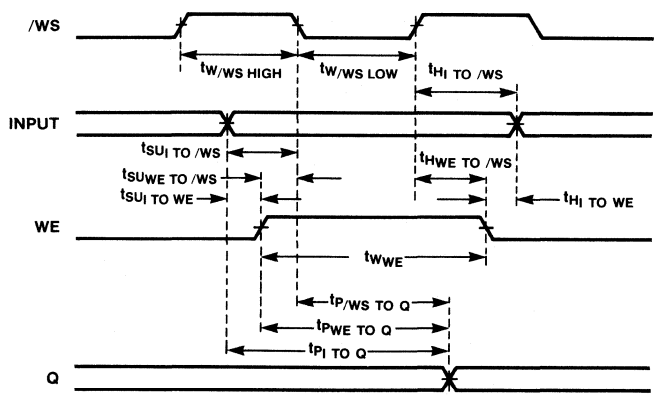
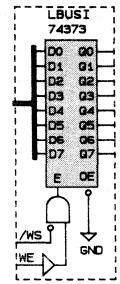


Figure 15D. LBUSI—Input Latch, Data from Internal Bus

Truth Table

/WS	WE	IB	Q	Q^+
L	H	L	X	L
L	H	H	X	H
H	X	X	L	L
H	X	X	H	H
X	L	X	L	L
X	L	X	H	H

IB—INTERNAL BUS



		EPB1400-2			EPB1400			
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
t_W	Pulse duration of /WS high		30			40		ns
	Pulse duration of /WS low		15			20		ns
	Pulse duration of WE		20			25		ns
t_{SU}	Internal Bus to /WS		3			5		ns
	WE to /WS		10			15		ns
	Internal Bus to WE		2			4		ns
t_H	Internal Bus to /WS		5			8		ns
	WE to /WS		2			4		ns
	Internal Bus to WE		5			8		ns
t_P	/WS to Q		6			9		ns
	WE to Q		8			12		ns
	Internal Bus to Q		6			9		ns

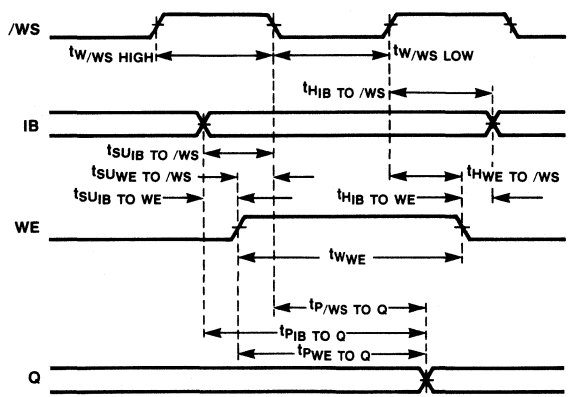
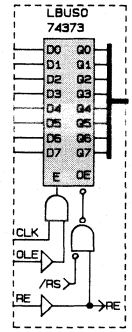


Figure 15E. LBUSO—Output Latch



Truth Tables

CLK	OLE	D	Q	Q^+
H	H	H	X	H
H	H	L	X	L
L	X	X	H	H
L	X	X	L	L
X	L	X	H	H
X	L	X	L	L

/RS	RE	Q	IB
L	H	H	H
L	H	L	L
X	L	X	Z
H	X	X	Z

IB—INTERNAL BUS

		EPB1400-2			EPB1400			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_W	Pulse duration of CLK		15			20		ns
	Pulse duration of OLE, RE		20			25		ns
	Pulse duration of /RS		20			25		ns
t_{SU}	Data to CLK		3			5		ns
	OLE to CLK		5			8		ns
	RE to /RS		8			12		ns
t_H	Data to CLK		3			5		ns
	OLE to CLK		1			3		ns
	RE to /RS		1			3		ns
t_P	Data to Internal Bus		6			10		ns
	CLK to Internal Bus		8			12		ns
	OLE to Internal Bus		12			16		ns
t_{PZX}	/RS to Internal Bus Valid		6			9		ns
	RE to Internal Bus Valid		9			14		ns
t_{PXZ}	/RS to Internal Bus Tri-state		5			8		ns
	RE to Internal Bus Tri-state		7			12		ns

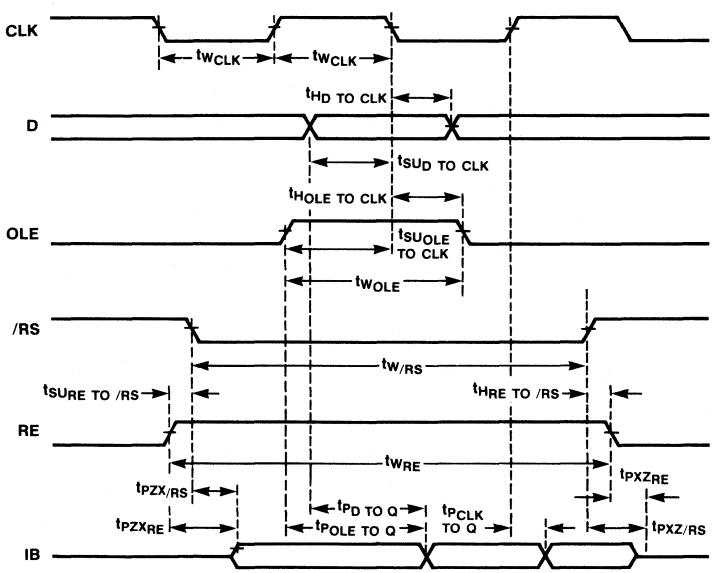
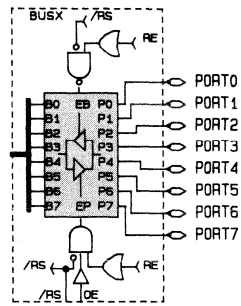


Figure 15F. BUSX—Bi-Directional Bus Port Transceiver

Truth Table

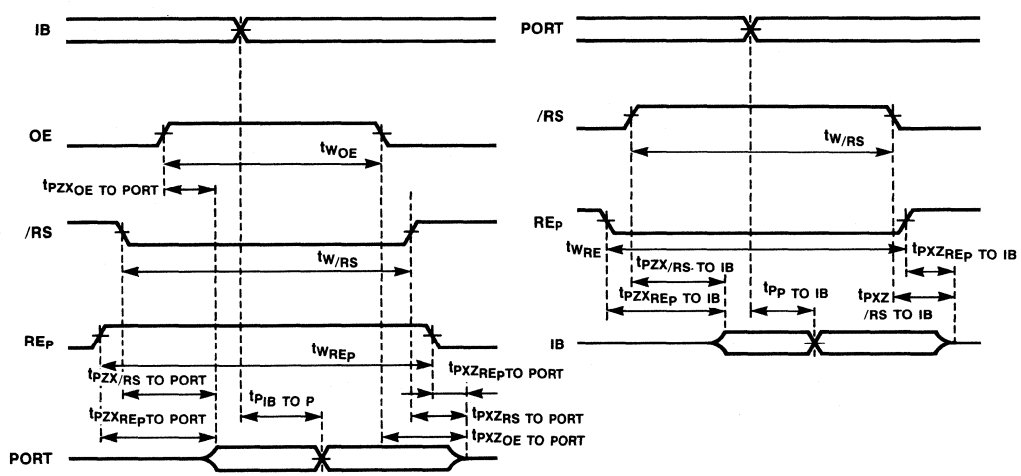
/RS	$RE_1 + RE_2$	OE	OPERATION
L	L	L	PORT DATA TO INTERNAL BUS
L	L	H	PORT DATA TO INTERNAL BUS
L	H	L	ISOLATION
L	H	H	INTERNAL BUS DATA TO PORT
H	L	L	PORT DATA TO INTERNAL BUS
H	L	H	PORT DATA TO INTERNAL BUS
H	H	L	PORT DATA TO INTERNAL BUS
H	H	H	PORT DATA TO INTERNAL BUS

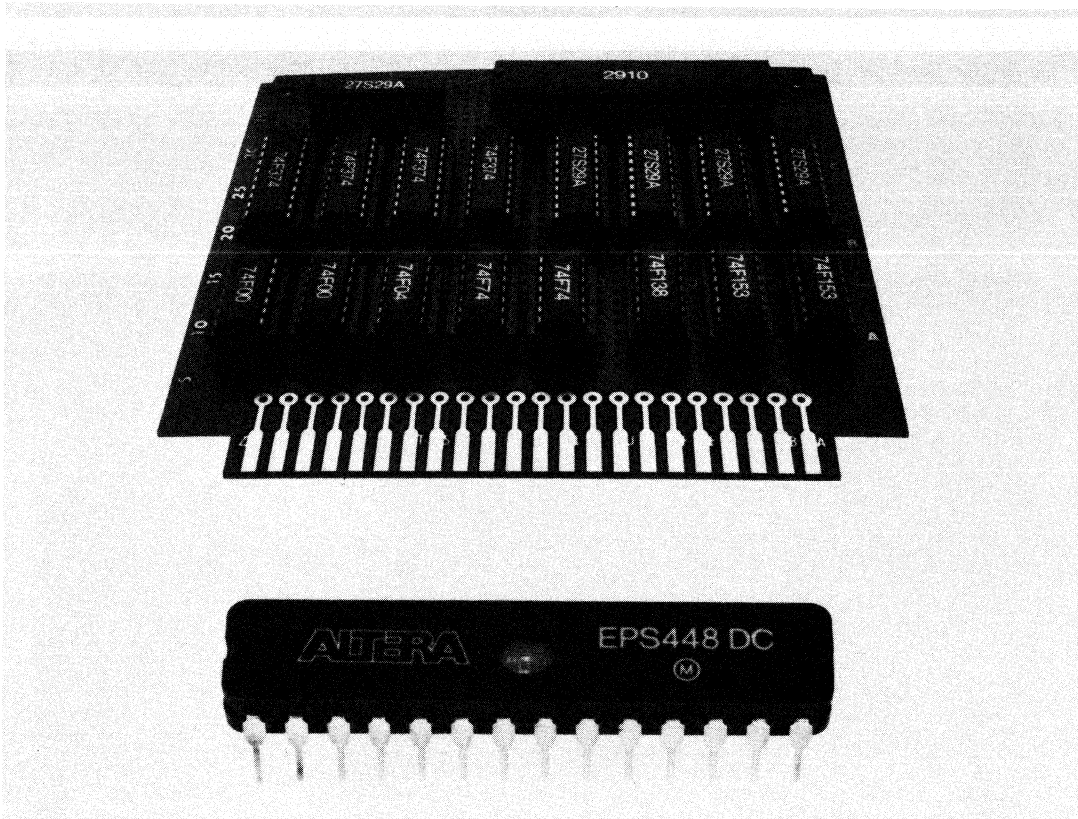
RE_1 = RE FOR SIDE 1 OUTPUT LATCH
RE_2 = RE FOR SIDE 2 OUTPUT LATCH
RE_P = RE FOR THE BUS PORT, RE_P IS THE LOGICAL "OR" OF RE_1, RE_2
IB = INTERNAL BUS



SYMBOL	PARAMETER	EPB1400-2 MIN	EPB1400-2 TYP	EPB1400-2 MAX	EPB1400 MIN	EPB1400 TYP	EPB1400 MAX	UNIT
t_P	Port to Internal Bus		4			6		ns
	Internal Bus to Port		15			20		ns
t_{PZX}	/RS to Port Valid		20			26		ns
	OE to Port Valid		18			24		ns
	RE to Port Valid		22			28		ns
	/RS to Internal Bus Valid		6			9		ns
	RE to Internal Bus Valid		9			14		ns
t_{PXZ}	/RS to Port Tri-state		15			20		ns
	OE to Port Tri-state		14			18		ns
	RE to Port Tri-state		16			22		ns
	/RS to Internal Bus Tri-state		5			8		ns
	RE to Internal Bus Tri-state		7			12		ns

Note:
For parameters related to Bus Port outputs, load capacitance is 100pF. (C_1 = 100pF, Figure 12)




27S29A
2910
74F00
74F04
74F74
74F138
74F153
ALTERA
EPS448 DC

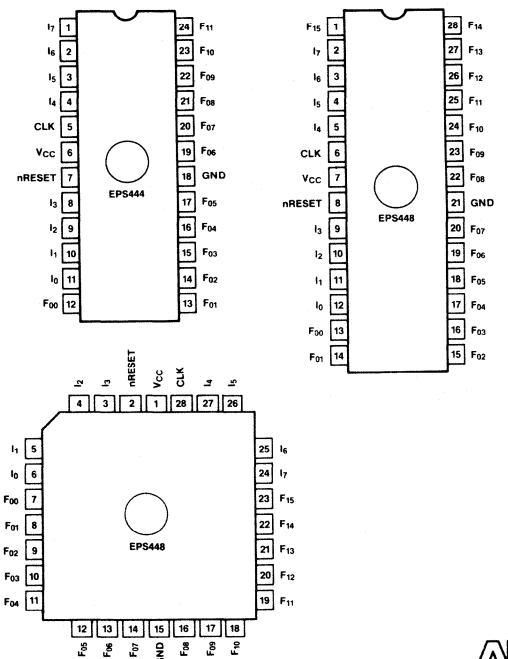
EPS444
EPS448

STAND-ALONE MICROSEQUENCERS

FEATURES

- User-Configurable/Stand-Alone Microsequencer (SAM) for implementing high-performance controllers
- On-Chip reprogrammable EPROM Microcode Memory up to 448 words deep
- 15 x 8 Stack
- Loop Counter
- Prioritized, multi-way Control Branching
- 8 general-purpose Branch Control Inputs
- 12 (EPS444) or 16 (EPS448) general-purpose Control Outputs
- Cascadable to expand outputs or states
- Low-Power CMOS technology
- Footprint Efficient 24/28 pin 300 Mil DIP or 28 lead JLCC/PLCC package
- 30 MHz Clock Frequency — typical
- Serial Scan Path testing capability
- High Level IBM-PC or compatible Design Support Software (SAM+PLUS):
  - State Machine Input Language (ASMILE)
  - Microcode Assembler
  - Functional Simulator

CONNECTION DIAGRAM



GENERAL DESCRIPTION

Altera's EPS44x (SAM) series of Function-Specific CMOS EPLDs are User-Configurable Microsequencers. On-chip EPROM (up to 448 words) is integrated with Branch Control Logic, Pipeline Register, Stack, and Loop Counter. This generic microcoded architecture provides an efficient vehicle for implementing a broad range of high performance controllers spanning the spectrum from basic state machines to traditional bit-slice controller applications.

Two versions of the SAM device are initially available: EPS444 and EPS448. Each device has eight general purpose input pins, a clock pin and a reset pin. The number of outputs and package options are key differences. The EPS444 has 12 user-definable outputs packaged in a 24-pin 300 mil DIP package. The EPS448 has 16 output pins available in a 28-pin 300 mil DIP package as well as a 28-pin JLCC option. One-Time-Programmable plastic versions for each SAM EPLD are available to minimize volume production costs.

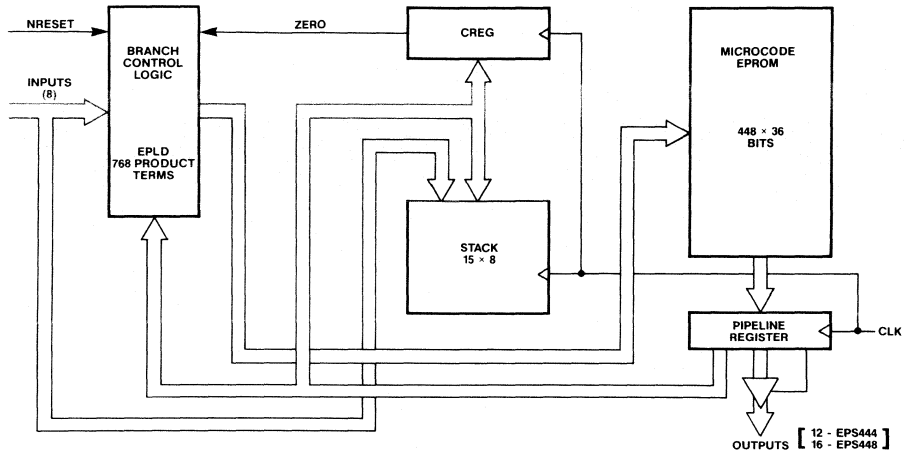
Programming the SAM device is accomplished on a standard Altera PLDS or PLCAD development system installed with the optional SAM+PLUS software package and device adapters. New users can purchase a separate PLDS-SAM development system with programming hardware included. SAM+PLUS allows designs to be entered in either state machine or microcoded formats. SAM+PLUS automatically performs logic minimization and design fitting for the device. The design may then be simulated or programmed directly to achieve customized working silicon within minutes.

PRELIMINARY DATA

NOTICE: THIS IS NOT A FINAL SPECIFICATION. SOME PARAMETRIC LIMITS ARE SUBJECT TO CHANGE.

REV. 1.2

Figure 1. EPS44x Block Diagram



Using a 1.0 micron CMOS EPROM technology allows SAM to operate at a 30 MHz typical clock frequency while still enjoying the benefits of low CMOS power consumption. This technology also facilitates 100% generic testability which eliminates the need for post-programming testing.

Ideal application areas for SAM include programmable sequence generators (state machines), bus and memory control functions, graphics and DSP algorithm controllers, and other complex, high performance machines. The devices may be cascaded easily to obtain greater output requirements (horizontal cascade) or greater microcode memory depth (vertical cascade) or both.

SAM AS A STATE MACHINE

The SAM architecture allows easy implementation of synchronous state machines. SAM's internal EPROM memory together with its Pipeline Register allows storage of up to 448 unique states. SAM's Branch Control Logic allows single clock, multiway branching in response to the eight inputs, current device state, and user-defined transition conditions. Design entry is simplified with Altera's State Machine Input Language (ASMILE) supported by the SAM+PLUS development system. This high level language uses IF-THEN-ELSE statements to define state transitions and a truth table to define or tri-state the outputs on a state-by-state basis.

SAM AS A MICROCODED CONTROLLER

SAM's architecture has several advanced features that enable it to be used as a complex microcoded controller. SAM's on-chip EPROM (448 words) is integrated with a microcode sequencer consisting of Branch Control Logic, Stack, and Loop Counter. The eight general-purpose inputs, the Counter, the Stack, and the Pipeline Register feed the Branch Control Logic. The Branch Control Logic gives flexible multi-way microcode branch capability in a single clock, enhancing throughput beyond that of conventional controllers or sequencers.

SAM+PLUS development software offers high level microcode entry featuring a compact assortment of powerful instructions (OP-codes) allowing easy implementation of conditional branches, subroutine calls, multiple level for-next loops, and dispatch functions (branching to an externally specified address).

FUNCTIONAL DESCRIPTION

The SAM architecture is shown in Figure 1. The primary elements are the Microcode EPROM, 36-bit Pipeline Register, Branch Control Logic, 15 x 8-bit Stack, and 8-bit Loop Counter.

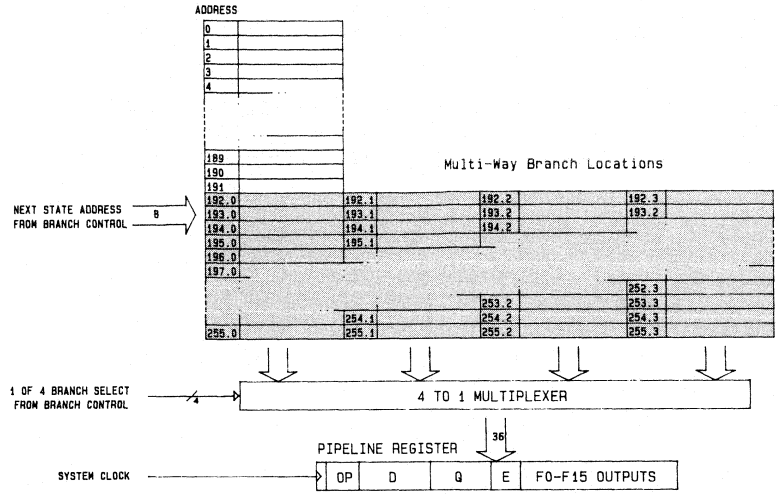
The Branch Control Logic generates the address of the next state and applies this address to the Microcode Memory. The outputs of the Microcode Memory represent the user-defined outputs and internal control values associated with the next state. On the leading edge of the clock these new values are clocked into the Pipeline Register and become the current state. The new values in the Pipeline Register—along with the Counter, Stack and Inputs—are used by the Branch Control Logic to generate the new next-state address.

MICROCODE EPROM & PIPELINE REGISTER

The Microcode EPROM is organized into 448, 36-bit words or locations, each of which can be viewed as a single state. Either 12 (EPS444) or 16 (EPS448) of these bits (the F-field) are available at device pins as user-defined outputs.

The other 20 bits are internal control signals that are divided into 4 fields: the 8-bit Q-field normally provides the next-state address; the 8-bit

Figure 2. SAM Microcode Memory



D-field is a general purpose field used either as a constant or as an alternative next-state address; the OP-field contains the instruction; and, the E-field contains a single bit which enables or tri-states the device outputs.

As shown in Figure 2, the Microcode Memory is organized as 256 rows or addresses. Addresses 0 through 191 contain a single 36-bit word which is associated with the desired next-state. This state information will be clocked into the Pipeline Register on the next rising edge of the clock and the outputs will become valid one T_{co} (clock to output delay) later.

Addresses 192-255, on the other hand, access 4 unique 36-bit words which correspond to 4 possible next states. (The extension .0, .1, .2, and .3 are used to distinguish those 4 states). These 64 addresses are known as Multiway Branch locations and are used to perform single clock 4-way branches. Whenever the next-state address falls within the Multi-Way Branch locations, the Branch Control Logic will make the necesary 1-of-4 selection based on the next-state address and user-defined input conditions.

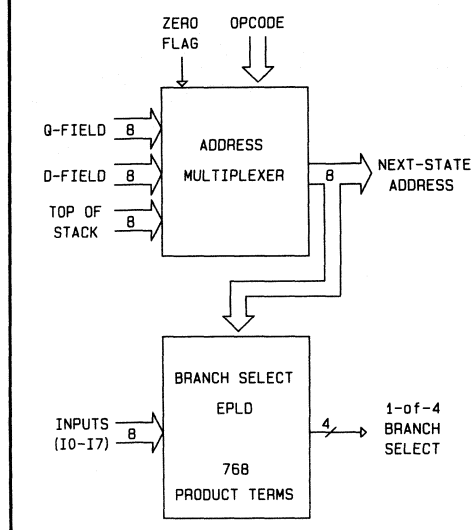
BRANCH CONTROL LOGIC BLOCK

At the heart of the high-performance sequencing ability of the SAM family is the Branch Control Logic. This block determines the next-state to be clocked into the Pipeline Register based on the current status of the Pipeline Register, the Counter, the Stack, and the eight input pins.

The Branch Control Logic is divided into two segments: the Address Multiplexer and the Branch Select EPLD.

The Address Multiplexer provides the next-state address to the Microcoded Memory. The next-state address can come from the Q-field, the D-field, or the Top of Stack. The selection between these three resources is based on the instruction in the Pipeline Register and the condition of the Zero Flag from the Counter.

Figure 3. SAM Branch Control Logic



The Branch Select EPLD is used to perform up to a 4-way branch based on user-defined input conditions. This block is a 768 product-term programmable logic device with 16 inputs and four outputs. When the next-state address falls within the multi-way branch block of memory (any address greater than 191) the Branch Select EPLD performs the necessary 1-of-4 selection. When the next-state address is less than 192, the Branch Select EPLD is turned off since no selection is required.

The conditions controlling the multi-way branch are defined by the user with a simple IF, THEN, ELSE format like the following.

```
      IF (cond3) THEN select 201.3
ELSEIF (cond2) THEN select 201.2
ELSEIF (cond1) THEN select 201.1
ELSE                select 201.0
```

The conditions are prioritized so that if the first condition is met (cond3), then microword 201.3 will be selected and clocked into the Pipeline Register regardless of the results of cond2 and cond1. If none of the three conditions are met, then the microword 201.0 will be clocked into the Pipeline Register.

The 3 conditional expressions are user defined and may contain any logical equation based on the inputs that can be reduced to 4 product-terms. For example, the expression

```
 I1 * /I2 * /I4
+I3 * /I4 * /I5 * /I6 * /I7
+I0
+I2 * /I4 * /I5
```

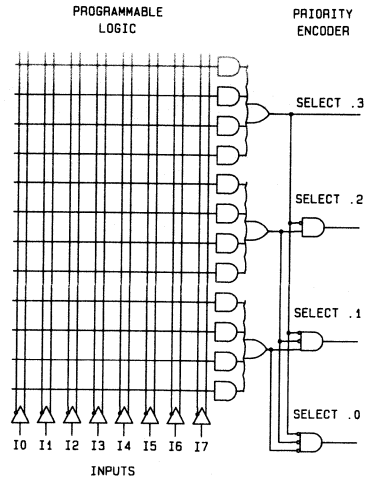
contains 4 product-terms and is a valid condition. There is a unique set of 12 product-terms for each of the 64 multi-way branch locations for a total of 768 product-terms. (See Figure 4).

The EPS44x has been designed so that the number of available product-terms should never be the limiting factor on a design. Prioritization provides an effective product-term count of more than 12 per location. A trade-off between number of product-terms and number of possible branches can be made by simply placing identical state information in two locations as shown in Figure 5.

STACK

The Stack of the EPS44x is a Last In First Out (LIFO) arrangement consisting of 15 8-bit words. The Top of Stack may be used as the next-state address or popped into the Counter. Values may be pushed onto the stack either from the D-field in the Pipeline Register or from the Counter which allows efficient implementation of subroutines, nested loops, and other iterative structures. The 8 input lines may also be pushed onto the stack to allow external address specification in a dispatch function or to externally load the counter.

Figure 4. SAM Branch Logic for Address 192



The PUSHing or POPing of the stack occurs on the leading edge of the clock. The stack is "zero filled" so that a POP from an empty stack will return all 8 bits set to zero. On the other hand, a push to an already full stack will write over the Top of Stack leaving the other 14 values unchanged.

LOOP COUNTER

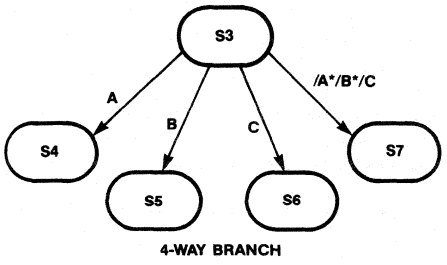
The EPS44x contains an 8-bit Loop Counter, referred to as the Count Register (CREG), which is useful for controlling timing loops and affecting a variety of branch operations. The CREG is a down counter and may be loaded directly from the D-field of the Pipeline Register or from the Top of Stack. The value of the CREG may be saved and restored by pushing and popping it to and from the Stack.

The CREG is loaded or decremented on the leading edge of the clock. It is designed so that it will not decrement once it reaches zero to prevent roll-over. A Zero Flag indicates when the counter has reached zero and is used with the LOOPNZ command to control program flow (see Instruction Set Description). Single instruction delay loops are easily constructed and, in combination with the Stack, nested loops or delays of arbitrary length may be generated.

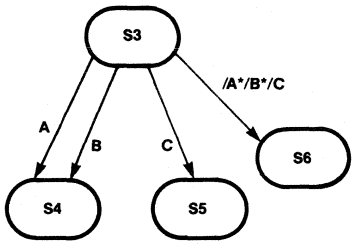
INSTRUCTION SET

The instruction set of the EPS44x consists of a compact assortment of powerful commands. Assembly language constructs allow efficient implementation of multi-way branching, subroutines,

Figure 5. Multi-Way Branching

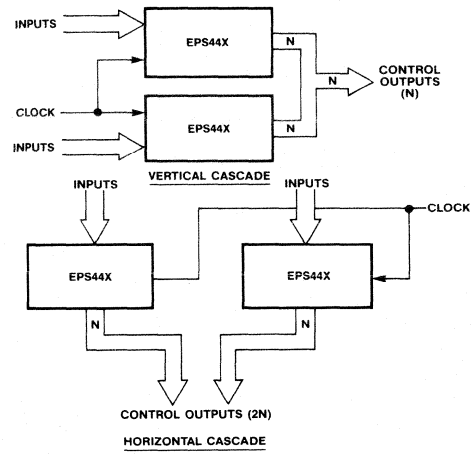


4-WAY BRANCH



3-WAY BRANCH

Figure 6. EPS44x Cascading



nested for-next loops, and dispatch functions. The complete instruction set is described at the end of this datasheet. These instructions are only used with assembly language design entry and are automatically supplied when using the Altera State Machine Input Language (ASMILE).

OUTPUT ENABLE CONTROL

Each microcode word contains an OE bit (the E-field) which enables the outputs when E = 1 and causes a high-impedance when E = 0. These bits are accessible through high-level constructs in the Altera Development Software. This capability allows the vertical cascading of EPS44x devices to increase the number of states.

nRESET PIN

The nRESET pin acts as a master reset for the EPS44x causing it to empty the Stack, clear the Counter, and load the microword found at address 0 into the Pipeline Register. The nRESET signal is useful for system reset or for synchronizing several SAMs that are cascaded vertically or horizontally.

The nRESET signal must be held low for at least three clock rising edges to perform a valid clear. A nRESET of one clock rising edge causes the EPS44x to enter into a supervisor mode (see SCAN TESTING below) and a nRESET of two clock edges results in an undefined state.

The outputs of the boot address (00 Hex) will appear at the pins from the fourth clock edge after nRESET goes low, until the third clock edge after nRESET returns to high.

HORIZONTAL AND VERTICAL CASCADING

Just as with memory and bit slice devices, the SAM devices can be cascaded to provide greater functionality. If an application requires more output lines, two or more SAMs can be cascaded horizontally. Likewise, if an application requires more states, two or more SAMs can be cascaded vertically. In either case, no speed penalty is incurred. Designs utilizing horizontal cascading are fully supported by the SAM+PLUS development software. Vertical cascading requires the designer to make certain tradeoffs to split the design.

AC SPECIFICATIONS

The timing specifications shown in the AC SPECIFICATIONS indicate typical timing values derived from design simulations. Worst case values will be provided after characterization of silicon. The minimum clock cycle (T_{cyc}) indicates the fastest that the part can be reliably run. At this speed it is guaranteed that all instructions will be executed in a single cycle.

FUNCTIONAL TESTING

The EPS44x is fully functionally tested and guaranteed through complete testing of each pro-

ABSOLUTE MAXIMUM RATINGS

COMMERCIAL
OPERATING RANGE

Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	With respect to GND note (2)	-2.0	7.0	V
V_{PP}	Programming supply voltage		-2.0	14.0	V
V_I	DC INPUT voltage		-2.0	7.0	V
I_{CCMAX}	DC V_{CC} or GND current		-200	200	mA
I_{OUT}	DC OUTPUT current, per pin		-25	+25	mA
P_D	Power dissipation			1100	mW
T_{STG}	Storage temperature	No bias	-65	+150	°C
T_{AMB}	Ambient temperature	Under bias	-10	+85	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage		4.75	5.25	V
V_I	INPUT voltage		0	V_{CC}	V
V_O	OUTPUT voltage		0	V_{CC}	V
T_A	Operating temperature		0	70	°C
t_R	INPUT rise time			500	ns
t_F	INPUT fall time			500	ns

DC OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3		0.8	V
V_{OH}	HIGH level TTL output voltage	I_{OH} = -8mA DC	2.4			V
V_{OH}	HIGH level CMOS output voltage	I_{OH} = -4mA DC	3.84			V
V_{OL}	LOW level TTL output voltage	I_{OL} = 8mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND			±10	μA
I_{OZ}	3-state output off-state current	$V_O = V_{CC}$ or GND			±10	μA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND I_O = 0 CLK = V_{CC}		65		mA
I_{CC2}	V_{CC} supply current (active)	No load 50% CLK f = 20 MHz		130		mA

CAPACITANCE

Note (3)

SYMBOL	PARAMETER	CONDITIONS	TYP	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1.0 MHz	30	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1.0 MHz	30	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V f = 1.0 MHz	30	pF
C_{RST}	nRESET Pin Capacitance		180	pF

AC CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)

			EPS44X-3			EPS44X-2			
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{CYC}	Maximum frequency	Load capacitance = 35pF		30			20		MHz
t_{CYC}	Minimum clock cycle			33			50		ns
t_{SU}	Input setup time			15			18		ns
t_H	Input hold time			0			0		ns
t_{CO}	Clock to output delay			15			20		ns
t_{CZ}	Clock to output disable or enable			15			20		ns
t_{CL}	Minimum clock low time			15			20		ns
t_{CH}	Minimum clock high time			10			15		ns
t_{SUR}	nRESET setup time			15			18		ns
t_{HR}	nRESET hold time			0			0		ns

Notes:
1. Typical values are for T_A = 25°C, V_{CC} = 5V
2. Minimum DC input is -0.3V. During transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
3. Capacitance measured at 25°C. Sample tested only.
4. If the nRESET is held low for more than 3 clock edges, then the outputs associated with the boot address (00 Hex) will remain at the pins until the third clock edge after nRESET goes high.

These preliminary specifications are provided for evaluation purposes. Conservative values are shown prior to full device characterization. Please request a copy of the current EPS444/448 Electrical Specification for complete information.
A Military Product Drawing will be prepared, in accordance with appropriate military specification formats, to provide guidance for the preparation of source control drawings (SCD).

Figure 7. Timing Waveforms

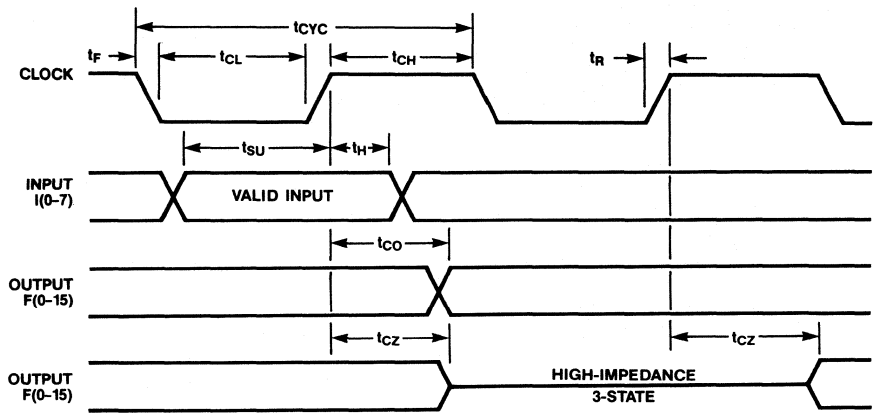
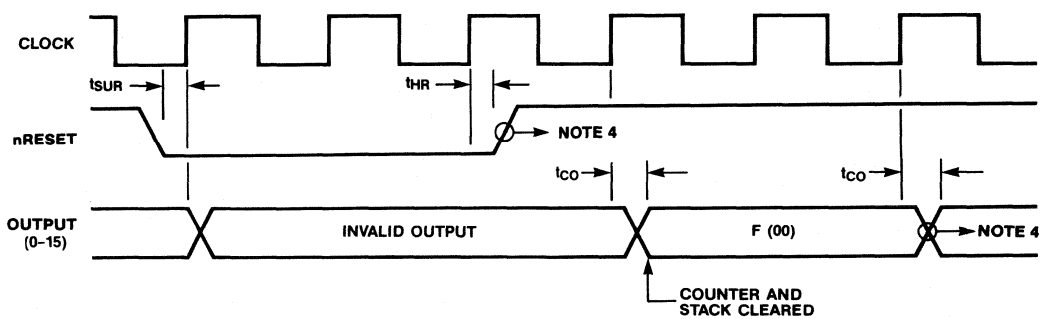


Figure 8. Reset Timing Waveforms



grammable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

The erasable nature of the EPS44x allows test programs to be used and then erased during early stages of production flow. This facility to use application-independent, general purpose tests is called generic testing and is unique among user-defined LSI logic devices. The devices also contain on board test circuitry to allow verification of function and AC specification once encapsulated in non-windowed packages.

SCAN TESTING

In addition to the functional testing done in the factory, the EPS44x can go into a serial scan mode which provides in-system testability.

The serial scan mode enables an internal 65-bit shift register to shift out the values of the critical registers within the EPS44x. This facility allows users to shift out the current status of the machine for examination. In addition, users can shift in an initial condition, execute for a controlled length of time, and shift out the resulting state. While scan testing is ongoing, all unused output pins are tristate disabled.

DESIGN SECURITY

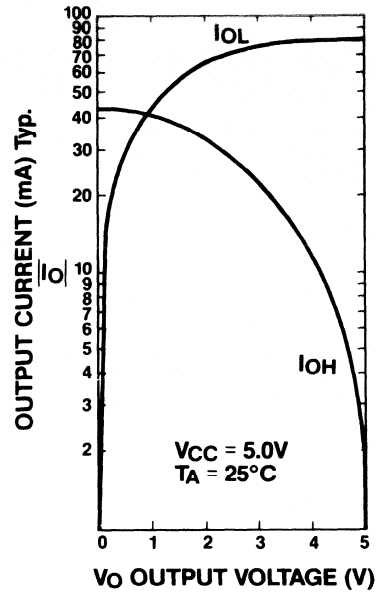
The EPS44X contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied nor retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

DESIGN RECOMMENDATIONS

Operation of the EPS44x with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. These devices contain circuitry to protect the input against damage to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

For proper operation, it is recommended that opaque labels be placed over the device window. Input and output pins must be constrained to the range GND $\leq$ (V_{in} or V_{out}) $\leq$ V_{cc}. Unused inputs must always be tied to an appropriate logic level (e.g. either V_{cc} or GND). A power supply de-

Figure 9. Output Drive Currents



coupling capacitor of at least 0.1 μF must be connected directly between the V_{cc} pin and GND.

When operating in noisy environments it is possible that a glitch on the nRESET pin one T_{sur} before the clock edge could initiate a supervisor mode. To prevent this possibility, it is recommended to connect a capacitor of at least 0.1 uF from the nRESET input to ground.

All general purpose inputs to the EPS44x should be synchronized to be guaranteed to meet the setup time. Input transitions which occur less than one T_{su} before the leading clock edge can cause the EPS44x to enter an undefined state.

INSTRUCTION SET DESCRIPTION

Following is a description of the instruction set available with the EPS44x. These instructions can be used in conjunction with the Assembly Language entry to access the various features of the EPS44x. They are automatically supplied when using the Altera State Machine Input Language (ASMILE).

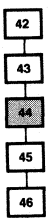
In the following description label1 and label2 indicate arbitrary labels located in the assembly (.ASM) file. These labels will be converted by the software into the 8-bit address of that label. The parameter constant is any 8-bit number (0-255

Decimal, 0-FF Hex) representing an address, a mask, or a constant.

The instructions influence the control of the Stack, the Counter, and the Address Multiplexer. These effects are summarized in the Instruction Table. Throughout the examples it is assumed for simplicity that the destination labels do not lie within the Multi-way Branch Block of memory so that branching based on inputs is not performed. It is valid, however, for any of these labels to lie within the Multi-Way Branch Block so that 4-way branching based on the inputs can be performed. See the MULTI-WAY BRANCH section at the end of this datasheet for more details.

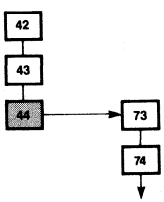
The SAM+PLUS development system allows the designer to use the high level Assembly Language without worrying about the actual values that are placed in the various fields.

CONTINUE



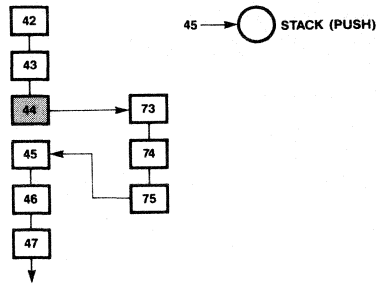
CONTINUE simply causes execution to continue with the next sequential instruction found in the Assembly Language file (.ASM).

JUMP label1



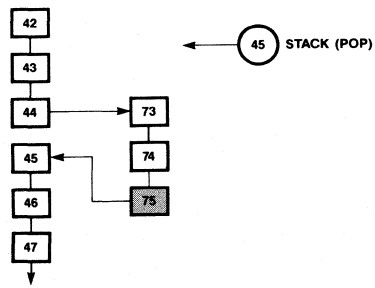
The JUMP instruction causes execution to branch to the indicated location. If address 44 contains the instruction 'JUMP label1,' then the next state will come from label1 which in this case is located at address 73.

CALL label1 RETURNTO label2



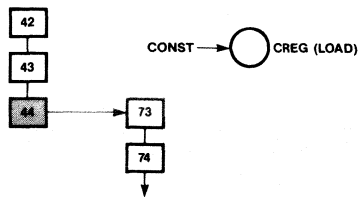
The CALL/RETURNTO instruction is typically used to call a subroutine. In general it will push the address of label2 onto the stack and cause label1 to be the next-state address. Leaving the RETURNTO designation off will cause label2 to default to the next instruction in the .ASM file. In the example, address 44 contains the command 'CALL label1' where label1 is located at address 73. This causes the address of the following instruction, in this case 45, to be pushed onto the stack, and the next state to come from address 73. The RETURN command at address 75 returns the execution to address 45.

RETURN



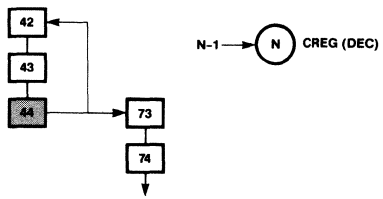
The RETURN command is used to return from a sub-routine call or in general to cause the next-state address to come from the top of stack. In the example, the command at address 44 CALLed the subroutine at address 73 and PUSHed the value 45 onto the stack. The RETURN command at address 75 will transfer execution to address 45 and POP that value off the stack.

LOADC constant GOTO label1



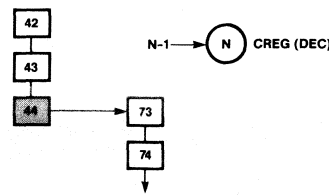
The LOAD Counter command loads the counter with the value specified and transfers execution to label1.The LOADC command is typically used to initialize the counter for a repetitive loop. In the example, address 44 has the command 'LOADC 173D GOTO label1' which causes the decimal value 173 to be loaded into the counter and the next state to come from label1. In this case label1 is located at address 73. If the GOTO designation is left off label1 will default to the next instruction in the .ASM file.

LOOPNZ label2 ONZERO label1



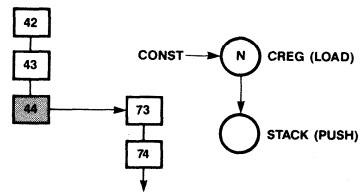
The LOOP on Non-Zero/ON ZERO goto command jumps to one of two addresses based on the value of the Zero Flag and decrements the Counter if not zero. This instruction is typically used to implement for-next loops. In the example, address 44 has the command 'LOOPNZ label2 ONZERO label1' where label2 is located at address 42 and label1 is located at address 73. If the Counter is not at zero then the next state will come from address 42 and the Counter will be decremented. If the Counter is already at zero then the instruction at address 73 will be executed and the Counter will stay at zero. If the ONZERO designation is left off, the default for label1 will be the next instruction in the .ASM file.

DECNZ GOTO label1



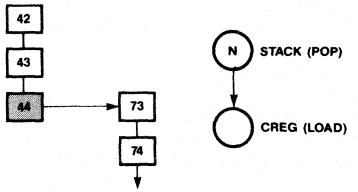
The DEcrement Counter on Non-Zero GOTO command will decrement the counter if it is non-zero and jump to label1. In the example, address 44 has the command 'DECNZ GOTO label1' where label1 is located at address 73. The Counter is decremented and the next instruction comes from address 73. The default for label1 is the next instruction in the .ASM file.

PUSHLOADC constant GOTO label1



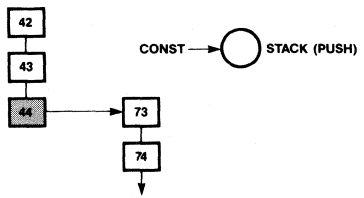
The PUSH counter LOAD Counter command will push the current value of the Counter onto the Stack, load a constant into the Counter, and jump to label1. This instruction is useful for implementing nested for-next loops. In the example, the instruction at address 44 is 'PUSHLOADC 153D GOTO label1' where label1 is located at address 73. The value in the counter will be pushed onto the stack, the decimal value 153 will be loaded into the counter, and the next instruction will come from address 73. The default for label1 is the next instruction in the .ASM file.

POPC GOTO label1



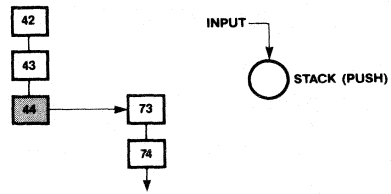
The POP stack to Counter GOTO command will pop the top of stack into the Counter and jump to label1. This command is typically used in conjunction with the PUSHLOADC to implement nested for-next loops. In the example, address 44 has the command 'POPC GOTO label1' where label1 is located at address 73. The default for label1 is the next instruction in the .ASM file.

PUSH constant GOTO label1



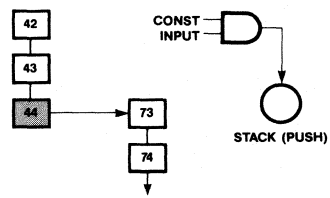
The PUSH constant to stack GOTO command will push the value constant onto the Stack and jump to label1. In the example, address 44 has the command 'PUSH 34D GOTO label1' where label1 is located at address 73. The decimal value 34 is pushed onto the Stack and the next state comes from address 73. The default for label1 is the next instruction in the .ASM file.

PUSHI GOTO label1



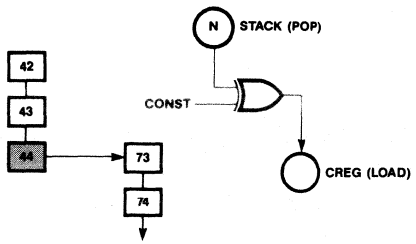
The PUSH Input GOTO command will push the eight inputs (I7-I0) onto the Stack. In the example address 44 has the instruction 'PUSHI GOTO label1' where label1 is located at address 73. At the leading edge of the clock the eight inputs are pushed onto the Stack. In a typical example, address 73 would have a RETURN instruction which would cause execution to jump to the address represented by the recently PUSHed input pins. This implements a dispatch function. The default for label1 will be the next instruction in the .ASM file. This instruction can also be used to load the Counter with an externally specified variable. In this case address 73 would have a POPC instruction.

ANDPUSHI constant GOTO label1



The AND PUSH Input GOTO command is identical to the PUSHI command except the inputs are first bit-wise ANDed with a constant. This allows the masking of irrelevant inputs before PUSHing an address for a dispatch routine.

POPXORC constant GOTO label1



The POP and XOR stack to Counter GOTO command will pop the top of Stack, bitwise XOR it with a constant, load the result into the Counter, and jump to label1. In the example, address 44 has the command 'POPXORC 25D GOTO label1' where label1 is located at address 73. The top of stack is POPed off the Stack, XORed with the decimal number 25, and loaded into the Counter. The next state comes from address 73. Since a XOR function does a comparison, this command can be used to compare the input to a constant and then branch based on the result with a LOOPNZ command. If the GOTO designation is left off the default for label1 will be the next instruction in the .ASM file.

MULTI-WAY BRANCHING

The multi-way branching capability can be super imposed upon the instruction set providing another dimension of capability. Figure 11 shows how this translates into the flow diagrams. If location 44 had the instruction 'JUMP label1' where label1 is located at address 201, then the next-state would come from address 201. But address 201 is within the Multi-Way Branch Block so the Branch Select EPLD must decide which of the 4 words to send to the pipeline register. This selection is based on user-defined functions of the inputs.

Similarly, location 44 could contain any of the 13 available commands so that the multi-way branch capability can enhance each instruction. If location 44 was a CALL to a subroutine, then address 201 could contain the starting instruction for 4 unique subroutines. The actual routine executed would depend on the condition of the inputs as defined by the user.

The actual Assembly Language code required to implement this example is as follows.

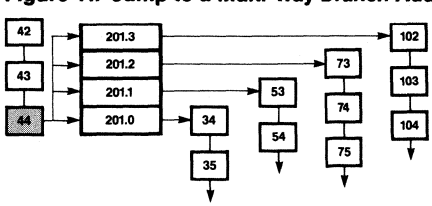
```
44D: [Output Spec] CALL label1;

201D: IF cond1 THEN [out 1] JUMP 102D;
ELSEIF cond2 THEN [out 2] JUMP 73D;
ELSEIF cond3 THEN [out 3] JUMP 53D;
ELSE [out 4] JUMP 34D;
```

Figure 10. Instruction Set Summary

INSTRUCTION	DEFINITION	NEXT-STATE ADDRESS	STACK	COUNTER
CONTINUE	Continue with next instruction	label1	None	HOLD
JUMP	Jump to a label	label1	None	HOLD
CALL	Call subroutine	label1	label2	HOLD
RETURN	Return from subroutine	STACK	POP	HOLD
LOADC	Load CREG	label1	None	constant
LOOPNZ	Loop/Dec. on Non Zero	label 1 or 2	None	DECREMENT
DECNZ	Decrement CREG on Non Zero	label1	None	DECREMENT
PUSHLOADC	Push CREG to Stack and Load CREG	label1	CREG	constant
POPC	Pop Stack to CREG	label1	POP	STACK
PUSH	Push constant to Stack	label1	constant	HOLD
PUSHI	Push inputs to Stack	label1	INPUTS	HOLD
ANDPUSHI	Push masked inputs to Stack	label1	INP * const	HOLD
POPXORC	XOR stack with constant and send result to CREG	label1	POP	STACK ⊕ constant

Note: The value label1 is placed in the Q-field. The values label2 and constant are placed in the D-field.

Figure 11. Jump to a Multi-Way Branch Address



ALTERA

EP1800JC-EV1 EVALUATION CHIP

EP1800 EVALUATION CHIP

- Erasable, User Configurable LSI circuit capable of implementing up to 2100 equivalent gates of custom and conventional logic.
- Pre-programmed to contain 14 MSI TTL functions for user evaluation.
- May be erased for other uses upon completion of evaluation.
- TTL/CMOS I/O compatibility.
- Design implemented using Altera's A+PLUS Development System
- Advanced CHMOS circuitry features low power, high performance, and high noise immunity
- Includes 68-pin JLCC ceramic package (window) and mounting socket.

The Altera EP1800JC-EV1 Evaluation EPLD provides a variety of logic functions for the purpose of evaluating the high density line of erasable programmable logic devices available from Altera.

The evaluation design contained in this application brief can be purchased as a pre-programmed EP1800 EPLD along with a suitable mounting socket for breadboarding. Ordering information is included at the end of this data sheet.

The EP1800 series of CHMOS EPLDs provide high performance, while at the same time, offering low power consumption, high noise margins, and ease of design. The EP1800 is implemented in a sub 2-micron dual-polysilicon CHMOS floating gate EPROM technology. The device supports a range of complexities up to 2100 equivalent 2-input NAND or NOR gates.

The speeds and density of the EP1800 series make it suitable for LSI replacement of Low power Schottky TTL in medium speed systems. It is also ideal for implementation of complete, high-performance functions such as special processors, dedicated peripheral controllers and intelligent support chips. IC count can be reduced by an order of magnitude depending on the system configuration. Power requirements can be reduced by several orders of magnitude, reliability significantly enhanced and the total size and cost of the system similarly reduced.

MACROCELLS

The internal logic arrays consist of programmable logic blocks each with its own I/O buffer. These blocks can be configured into a variety of logic elements such as exclusive-OR gates, AND gates, NAND gates, NOR gates, OR gates, latches and flip-flops. A single block is equivalent to over 40 2-input NAND gates. These elements are called MacroCells, and are the basic building blocks available to the designer. The EP1800 contains 48 MacroCells.

MACROFUNCTION LIBRARY

To specify the logic design, the user may use elements of greater complexity than a single MacroCell. These more complex elements are called MacroFunctions. They are composed of MacroCells. MacroFunctions may be combined within a single design to provide the complete specification of the required logic. Altera's MacroFunction library is a collection of high-level building blocks that can greatly increase design productivity. The initial library contains all the most commonly used TTL SSI and MSI functions. These aid the first time user since the function of these blocks will already be familiar.

The EPLD implementation of these MacroFunctions is contained in a standard TTL library designed for use with Altera's low cost schematic capture package LogiCaps.

These blocks can be used in combination with the existing gate and flip-flop primitives to provide a very rich design environment for EPLD logic development that contains over 180 logic functions.

The library also contains a number of more specialized MacroFunction blocks that perform powerful logic functions in an optimum manner for EPLD implementation. These blocks have been designed by EPLD design experts and contain inner logic behaviour optimized for speed and efficiency.

EVALUATION CHIP LOGIC

The EP1800-EV1 chip contains some 17 logic functions most of which are MacroFunctions. The overall configuration of the chip is shown in the final figure of this data sheet. The functions included are:

7485 — 4 bit magnitude comparator
74279 — quad S-R latch
74151 — 8 input multiplexer
74138 — 1 of 8 decoder
74157 — quad 2 input multiplexer
74194 — universal bidirectional shift register
74180 — 8 bit parity generator/checker
7483 — 4 bit full adder
74190 — up/down decade counter
7449 — BCD to 7 segment decoder
7474 — D type flip flop
74103 — JK type flip flop
7486 — Quad exclusive OR
Bidirectional bus interface

Most functions within the chip can be evaluated independently (an exception is the 74138 and 74157 which are evaluated in combination) so that each function and its performance can be thoroughly evaluated. For added breadboarding convenience the logic schematic has been drawn within an outline of the EPLD package. An actual design does not need to be implemented in this way.

In the following pages there are detailed logic diagrams (along with the LogiCaps Macro symbol and function table) for some of the MacroFunctions employed.

This evaluation design uses virtually all the I/O facilities of the EP1800 to allow maximum access to each function. However, the internal logic capabilities of this design employ only half of the available gate logic available in the chip.

This design can be compiled by the A+PLUS design processor in less than 10 minutes using a personal computer. A unique function built into the A+PLUS Design Processor ensures that the use of MacroFunction blocks causes no loss of design efficiency. The processor analyzes the complete logic circuit and automatically removes unused gates and flip-flops from any MacroFunction employed. This "MacroMuncher" process allows the logic designer to freely employ logic blocks without the headaches associated with optimizing their use. All inputs to MacroFunctions are defined with "intelligent" default input signal levels so that unused inputs to MacroFunctions can simply be left unconnected.

EP1800 DESIGN SUPPORT SERVICES

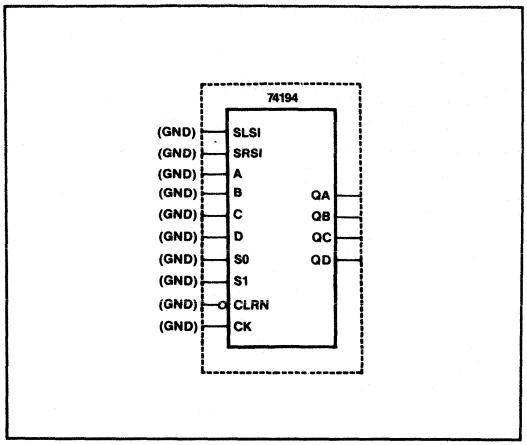
ALTERA provides design support services to augment the users design engineering capabilities.

Full design support is available for custom designs described in TTL schematic form. A complete set of design drawings and design compilation documentation is provided along with programmed functional devices. Typical turn-around is 5 to 10 working days depending on design complexity. Contact ALTERA marketing for details of typical design charges.

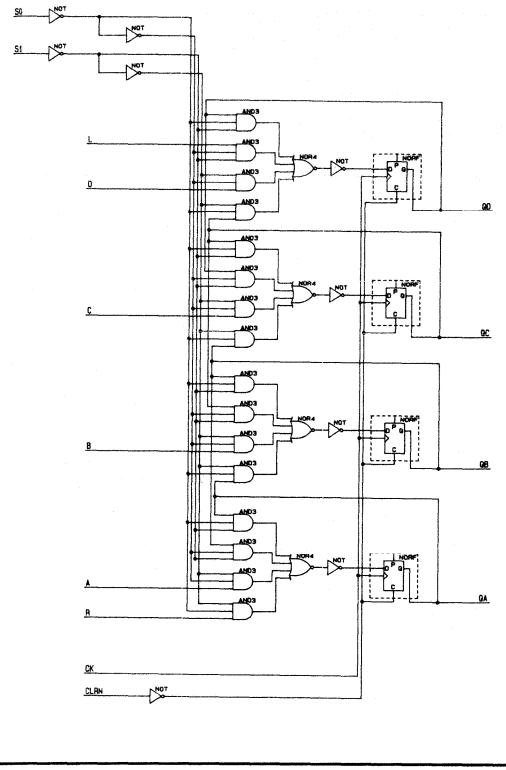
HOW TO ORDER

The EP1800-EV1 (chip and breadboarding socket) can be ordered directly from ALTERA. It comes complete with demonstration software diskettes for LogiCaps (ALTERA's EPLD schematic capture system) and the A+PLUS design compiler.

74194 (SHIFT REGISTER)



Logic Schematic:



Name: **74194** (4-Bit Bi-Directional Shift Register With Parallel Load)

Declaration: 74194(SL,SI,SRSI,A,B,C,D,R, S0,S1,CLRN,CK,QD,QC,QB, QA)

EPLDs: EP310, EP600, EP900, EP1210, EP1800

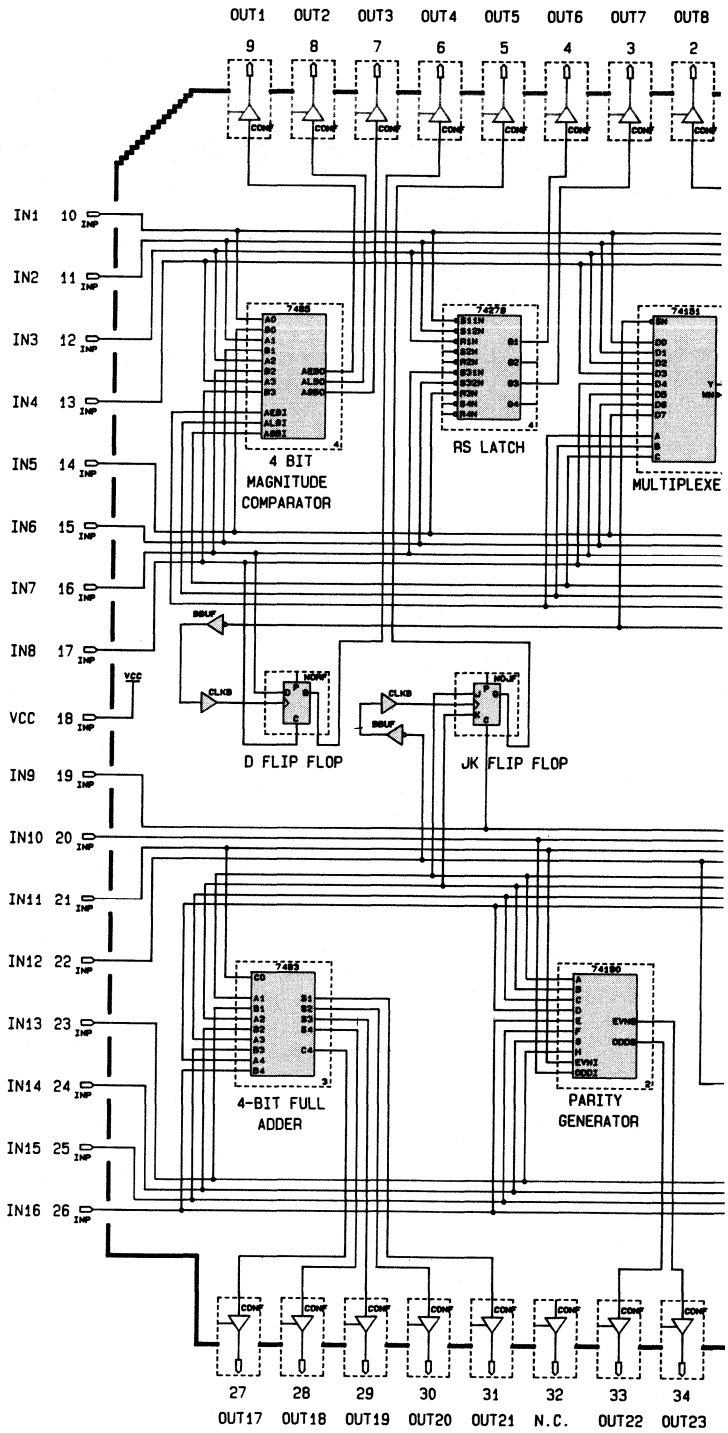
Default Signal Levels: GND—SLSI,SRSI,A,B,C,D,S0, S1,CK
VCC—CLRN

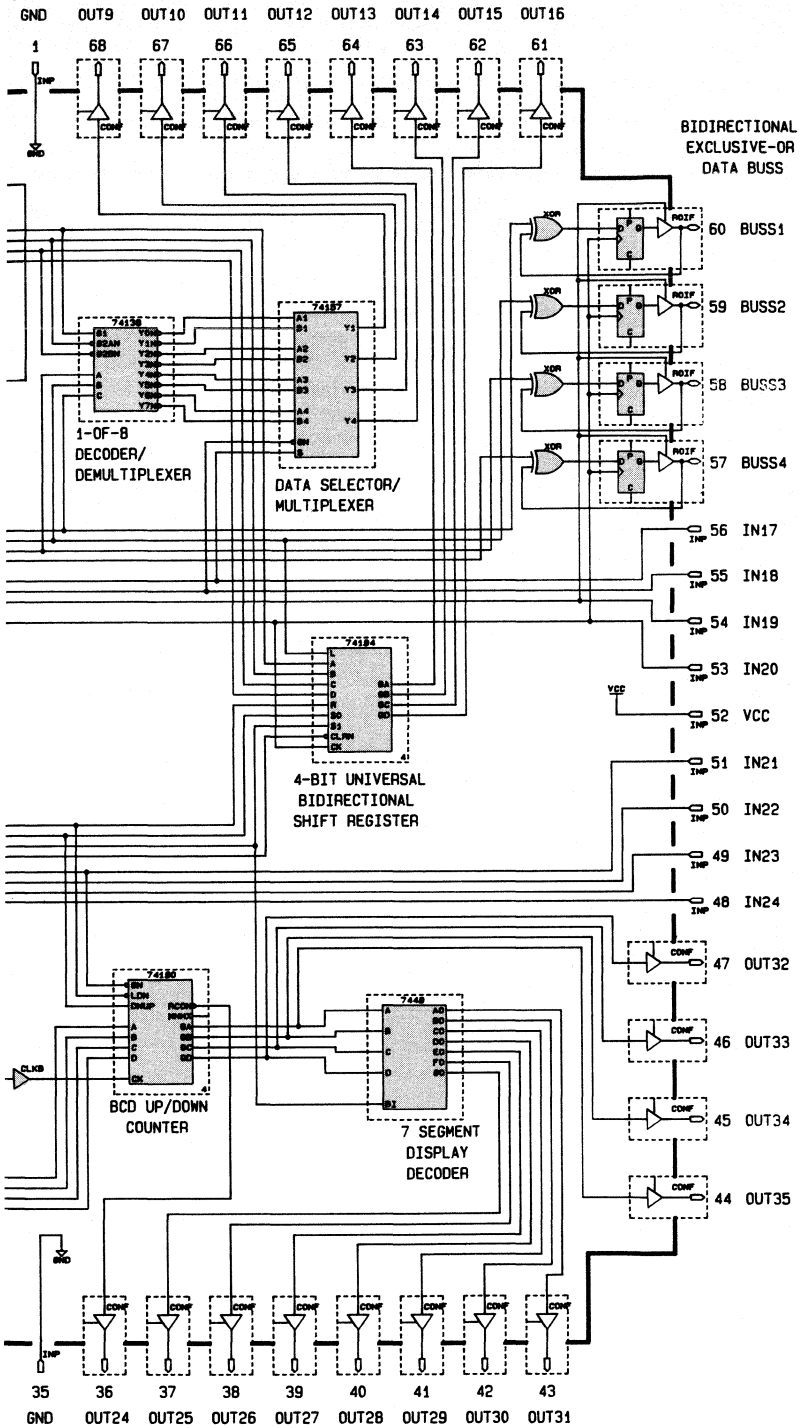
FUNCTION TABLE:

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		L	R	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	↑	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
↑ = transition from low to high level
a, b, c, d = level of steady state input at inputs A, B, C, D
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = level of Q_A, Q_B, Q_C, Q_D before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = level of Q_A, Q_B, Q_C, Q_D before the most recent ↑ transition of the clock.

EP1800JC-EV1
Evaluation Chip




GND
OUT9
OUT10
OUT11
OUT12
OUT13
OUT14
OUT15
OUT16
1
68
67
66
65
64
63
62
61
BIDIRECTIONAL
EXCLUSIVE-OR
DATA BUSS
60 BUSS1
59 BUSS2
58 BUSS3
57 BUSS4
56 IN17
55 IN18
54 IN19
53 IN20
52 VCC
51 IN21
50 IN22
49 IN23
48 IN24
47 OUT32
46 OUT33
45 OUT34
44 OUT35
1-OF-8
DECODER/
DEMULTIPLEXER
DATA SELECTOR/
MULTIPLEXER
4-BIT UNIVERSAL
BIDIRECTIONAL
SHIFT REGISTER
BCD UP/DOWN
COUNTER
7 SEGMENT
DISPLAY
DECODER
CLKB
35
GND
36
OUT24
37
OUT25
38
OUT26
39
OUT27
40
OUT28
41
OUT29
42
OUT30
43
OUT31

THE FOLLOWING DESIGN GUIDELINES AND RECOMMENDATIONS APPLY TO ALL EPLD COMPONENTS IN THIS DATA BOOK

PROGRAM ERASURE

The erasure characteristics of EPLDs are such that erasure of the programmed connections begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms. It is important to note that sunlight and certain fluorescent lighting could erase a programmed EPLD since they have wavelengths in the range of 3000 to 4000 Angstroms. Extrapolated results suggest that constant exposure to room level fluorescent lighting could erase an EPLD in approximately 3 years while it would take approximately 1 week to cause erasure when exposed to direct sunlight. As a consequence, if the EPLD is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the EPLD window to prevent unintentional erasure.

The recommended erasure procedure for EPLDs is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms. The integrated exposure dose for erasure should be a minimum of 15W/sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. EPLDs should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated exposure dose for an EPLD without damage is 7000 Wsec/cm^2. This is approximately one week at 12000 μW/cm^2. Exposure of EPLDs to high intensity UV light for long periods may cause permanent damage.

EPLDs may be erased and re-programmed as many times as needed using the recommended erasure exposure levels.

LATCH-UP & ESD PROTECTION

EPLD input, I/O and clock pins have been carefully designed to resist electrostatic discharge (ESD) and latch-up which are inherent to CMOS structures. Unless otherwise noted each of the EPLD pins will withstand voltage energy levels exceeding 1500 volts, per method specified by MIL STD 883C. The pins will not latch-up for input voltages between -1V to VCC + 1V with currents up to 100 mA. During transitions, the inputs may undershoot to -2.0V for periods less than 20 ns. Additionally, the programming pin is designed to resist latch-up to the 13.5 volt maximum device limit.

DESIGN RECOMMENDATIONS

Operation of devices described herein with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum rating condition for extended periods may affect device reliability. These devices contain circuitry to protect the input against damage to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

For proper operation, it is recommended that opaque labels be placed over device window. Input and output pins must be constrained to the range GND $\leq$ (V_{in} or V_{out}) $\leq$ V_{CC}. Unused inputs must always be tied to an appropriate logic level (e.g. either V_{CC} or GND). Each set of V_{CC} and GND pins must be shorted together directly at the device. Power supply decoupling capacitors of at least 0.1μF must be connected between each V_{CC} pin and GND. For the most effective decoupling, connect one capacitor between each set of V_{CC} and GND pins, directly at the device.

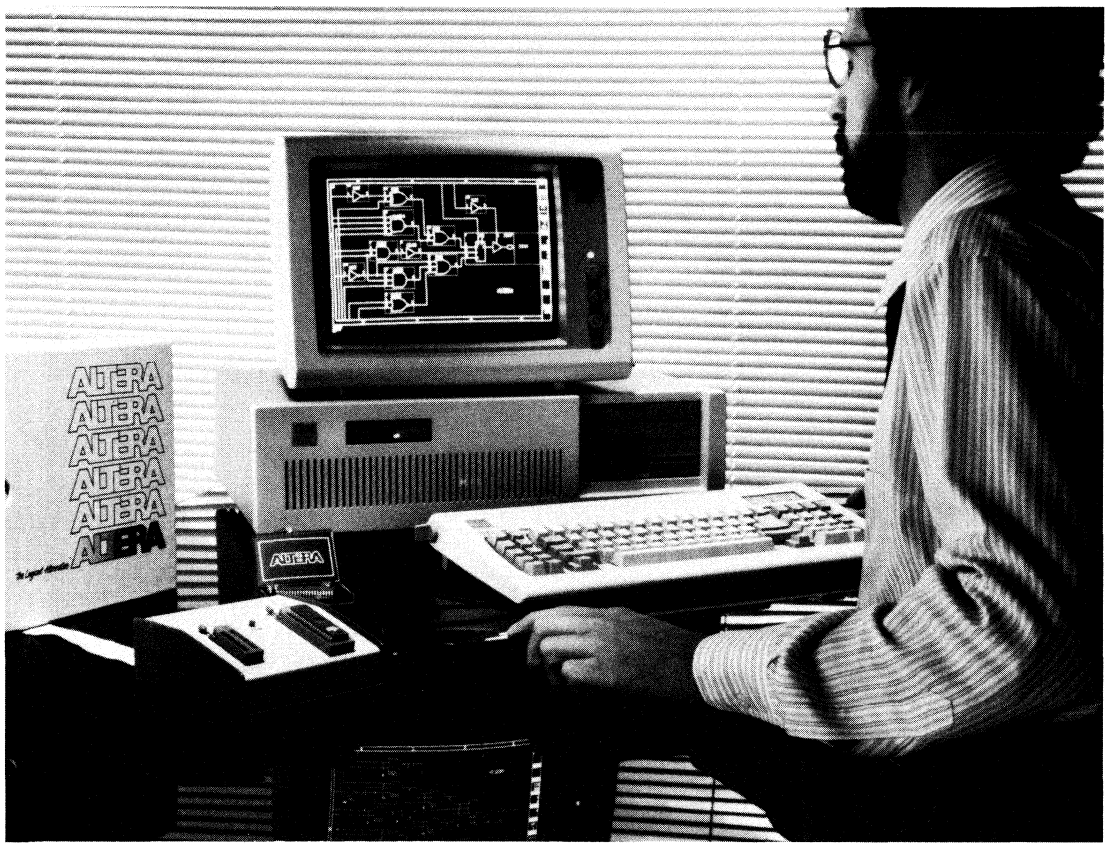
TURBO-BIT

Some EPLDs contain a programmable option to control the automatic power down feature that enables the low standby power mode of the device. This option is controlled by a TURBO-BIT which can be set using A+PLUS. When the TURBO-BIT is programmed (Turbo = ON), the low standby power mode (Icc1) is disabled. This renders the circuit less sensitive to Vcc noise transients which can be created by the power-up/power-down cycle when operating in the low power mode. The typical Icc vs frequency data for both Turbo and Non-Turbo (low power) mode is shown in each EPLD data sheet. All AC values are tested with the TURBO-BIT programmed.

If the design requires low power operation then the TURBO-BIT should be disabled (Turbo = OFF). When operating in this mode, some AC parameters are subject to increase. Values given in the AC specifications section under "Non-Turbo Adder" must be added to the respective AC parameter to determine worst-case timing.

DEVELOPMENT PRODUCTS DATASHEETS **PAGE NO.**

3

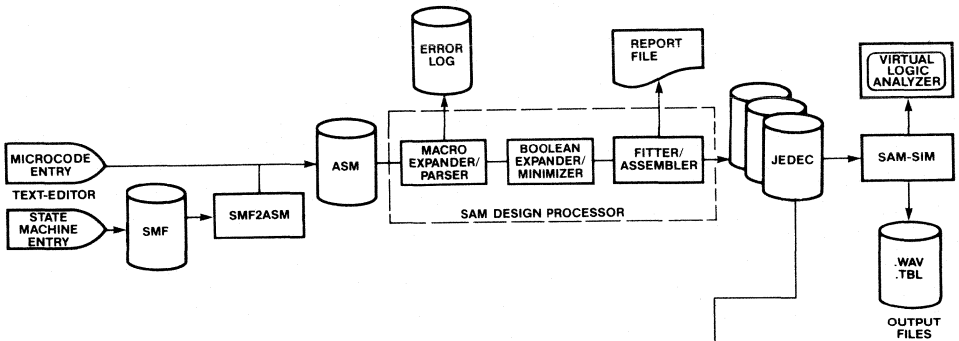


Installed on an IBM-XT, AT or compatible machine, Altera EPLD development tools provide a fast, flexible and easy to learn CAE development environment.

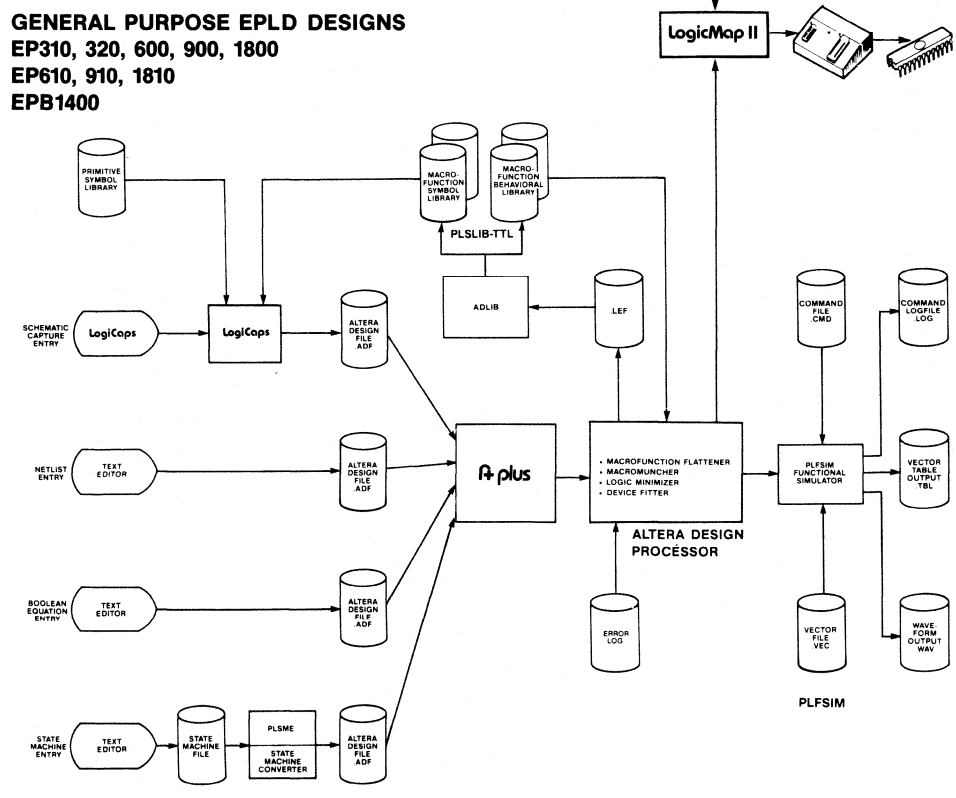
They may be purchased as complete development systems or as individual software and hardware products.

EPLD designs may be entered in many convenient formats. These include schematic capture (basic gates through TTL MacroFunctions), Boolean equations, State Machine and microcode assembler entry. Design Compilation performs logic minimization, automatic device fitting and generation of programming data in the standard JEDEC format. Device fitting is the PLD equivalent to an automatic place and route capability and is accomplished on a typical design in minutes. Design verification and device programming capabilities are also available. Altera development systems permit the use of many third party software and hardware products via appropriate interface programs.

STAND ALONE MICROSEQUENCER DESIGNS
EPS444, 448



GENERAL PURPOSE EPLD DESIGNS
EP310, 320, 600, 900, 1800
EP610, 910, 1810
EPB1400



3

PROGRAMMABLE LOGIC DEVELOPMENT SYSTEM WITH BOOLEAN EQUATION AND NETLIST ENTRY

PLDS2

PLDS2 CONTENTS

HARDWARE

- Software Controlled Programmer Interface Card, PLP4.
- EPLD Master Programming Unit, PLE3-12. Permits direct programming of Altera EP3XX (20 Pin) & EP12XX (40 Pin) devices.
- Two sample EPLDs for evaluation.

DOCUMENTATION

- A+PLUS reference manual.

SOFTWARE

- PLS2—A+PLUS programs and support files.
  - — ADP - Altera Design Processor.
  - — LogicMap - LogicMap Programming File.
  - — INSTALL - Installation Procedures.

SOFTWARE WARRANTY

- PLAESW-PC, 12-month extended software warranty & update service.

ORDER INFORMATION

PLDS2

GENERAL DESCRIPTION

The Altera PLDS2 (Programmable Logic Development System) is a complete hardware and software solution that enables circuit designers to develop and implement custom logic circuits with Altera EPLDs. The system contains A+PLUS, Altera Programmable Logic User Software, which allows a wide variety of design input methods that suit the particular logic design task. These include Netlist, Boolean Equation, optional Schematic Capture, and optional State Machine design entries. A+PLUS includes a Design Processor which transforms the input format to optimized code used to program the targeted EPLD.

The Design Processor implements logic minimization, automatic EPLD part selection, architecture optimization, and design fitting. A+PLUS also allows MacroFunction design capability and functional simulation. In addition to A+PLUS, the PLDS2 system also contains a programming card and master programming unit used for device programming. The programming card fits into the expansion slot of the PC and connects via ribbon cable to the master programming unit. The programming hardware is fully software controlled via A+PLUS.

REV. 3.0

PROGRAMMABLE LOGIC DEVELOPMENT SYSTEM — WITH SCHEMATIC CAPTURE DESIGN ENTRY PLCAD4

PLCAD4 FEATURES

- Fully Integrated Development System for all Altera general purpose EPLDs featuring LogiCaps Schematic Capture and A+PLUS (Altera Programmable Logic User Software).
- Supports Schematic Capture, Boolean Equation and Netlist design entry methods.
- 7400 Series Design Library allows for high-level design entry.
- Design flattening and logic minimization for complete optimization of the EPLD design.
- Intelligent fitting algorithm allows automatic EPLD part selection and pin assignments.
- Includes programming card and unit for direct device programming.
- Runs on IBM XT, AT or Compatible computers.

PLCAD4 CONTENTS

- Complete PLDS2 System.
- PLE40, LogiCaps Schematic Capture Software.
- PLSLIB-TTL MacroFunction Library.
- PLAESW-PC, 12 Month Extended Software Warranty and Update Service.

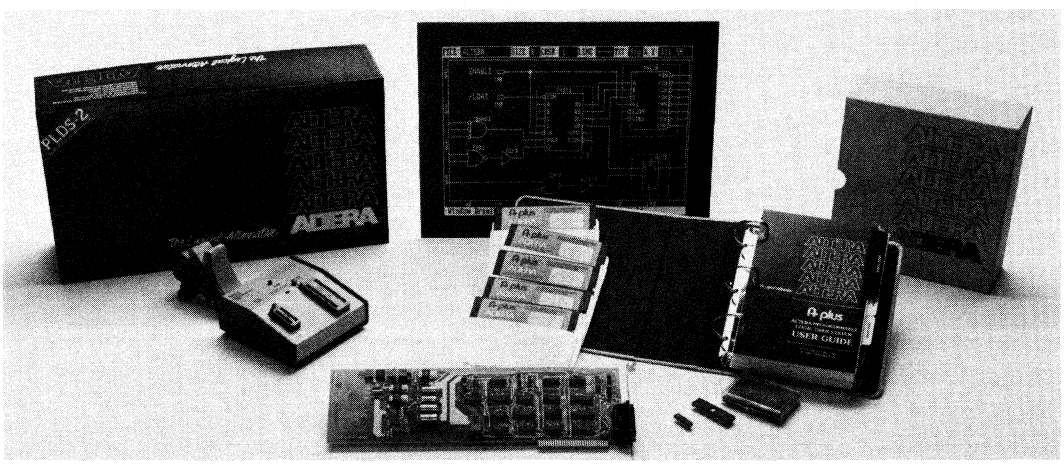
GENERAL DESCRIPTION

The Altera PLCAD4 EPLD Development System provides the ideal desktop environment for EPLD design entry, design compilation and fitting. PLCAD4 also includes EPLD programming hardware and software that can be used for direct device programming.

The primary method of design entry is LogiCaps, Altera's high performance schematic capture software. Using the TTL MacroFunction Library, along with LogiCaps, designers are able to draw their logic with familiar 7400 series devices. Once the schematic is completed, a single keystroke transforms the drawing into a design format, Altera Design File, ready for processing by A+PLUS.

ORDER INFORMATION

PLCAD4



REV. 3.0

PROGRAMMABLE LOGIC DEVELOPMENT SYSTEM SUPREME

PLCAD-SUPREME

PLCAD-SUPREME CONTENTS

- Complete PLDS2 System.
- PLE40, LogiCaps Schematic Capture Software.
- PLSLIB-TTL, TTL MacroFunction Library.
- PLSME, State Machine Entry Software.
- PLFSIM, Functional Simulation Software.
- PLED600, EP600/EP610 DIP Adapter.
- PLED900, EP900/EP910 DIP Adapter.
- PLEJ1800, EP1800J-Lead Adapter.
- PLAESW-PC, 12-Month Software Warranty and Update Service.
- Device Samples: EP320DC, EP1210DC, EP600DC, EP900DC, EP1800JC.

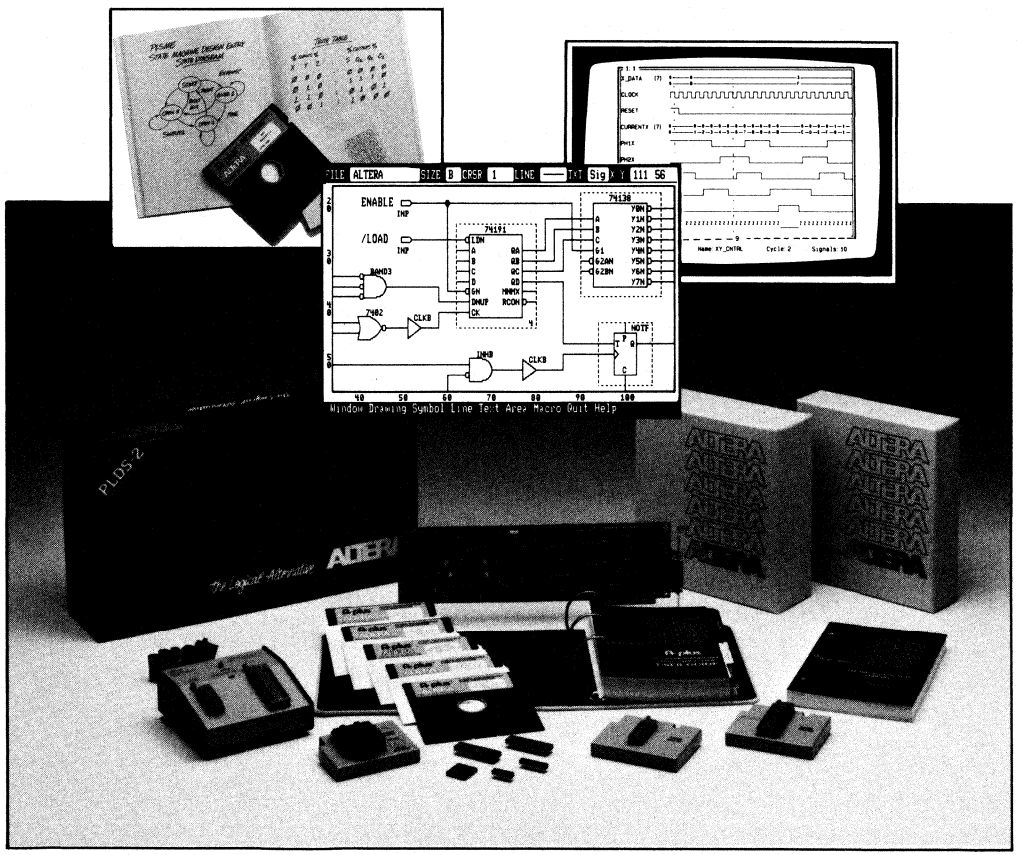
PLCAD-SUPREME contents may be purchased separately.

GENERAL DESCRIPTION

PLCAD-SUPREME provides all of the items contained within the PLDS2 system, plus additional software applications required for design entry and design verification. Also included is a master programming unit, various adapters, and device samples. PLCAD-SUPREME provides for complete design functionality across the full range of Altera general purpose EPLDs at a discounted price from purchasing each individual item separately.

ORDER INFORMATION

PLCAD-SUPREME



REV. 1.0

PROGRAMMABLE LOGIC DEVELOPMENT SYSTEM-SAM PLDS-SAM

PLDS-SAM CONTENTS

HARDWARE

- Software Controlled Programmer Interface Card.
- EPLD Master Programming Unit.
- PLED448 Programming Adapter for DIP EPS448 and EPS444 Devices.
- EPS448 Sample Device For Evaluation.

SOFTWARE

- PLS-SAM—SAM+PLUS programs and support files.
  - — SAM Design Processor.
  - — SAMSIM, Functional Simulator.
  - — LogicMap - LogicMap Programming and Support Files.

DOCUMENTATION

- SAM+PLUS Reference Manual.

ORDER INFORMATION

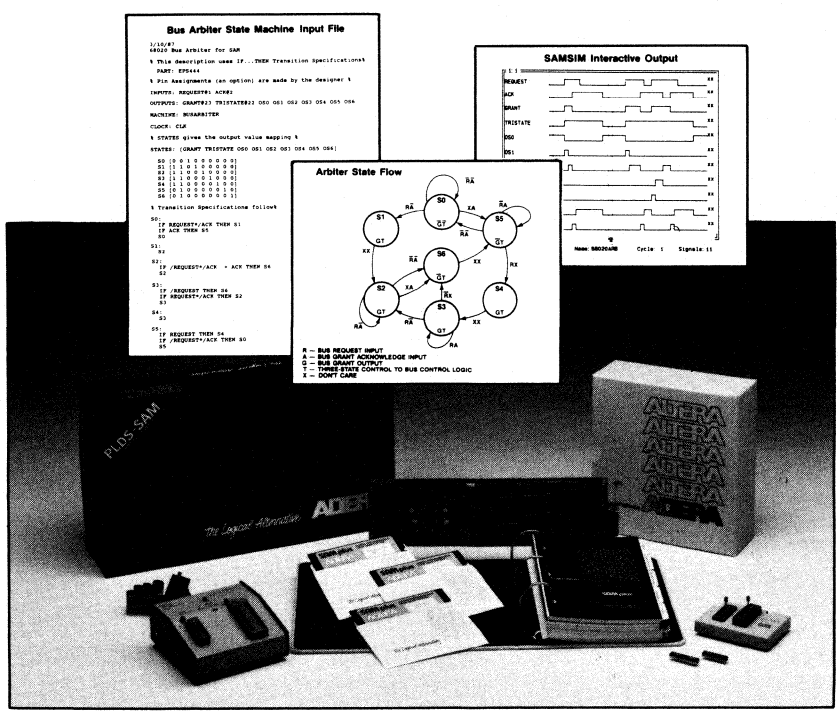
PLDS-SAM

GENERAL DESCRIPTION

The Altera PLDS-SAM (Programmable Logic Development System) represents a complete software and hardware solution to implementing State Machine and Microcoded applications into Altera's SAM family of Function-Specific EPLDs. PLDS-SAM is a comprehensive, easy to use system that encompasses design entry with SAM+PLUS, design debugging with SAMSIM, and device programming with the Altera programming hardware.

The SAM+PLUS processing software accepts two forms of design entry, State Machine and assembly language, and automatically generates an industry standard JEDEC file. SAMSIM is an interactive functional simulator created specifically for verification of State Machine and Microcoded designs implemented in SAM EPLDs. The programming hardware consists of an Altera programming card, a Master Programming Unit, and programming adapter for programming the SAM EPLDs.

For existing Altera PLDS or PLCAD users, PLS-SAM (Programmable Logic Software) is available as a software enhancement to their current system.



REV. 2.0

A+PLUS PROGRAMMABLE LOGIC USER SOFTWARE

PLS2 PLS4

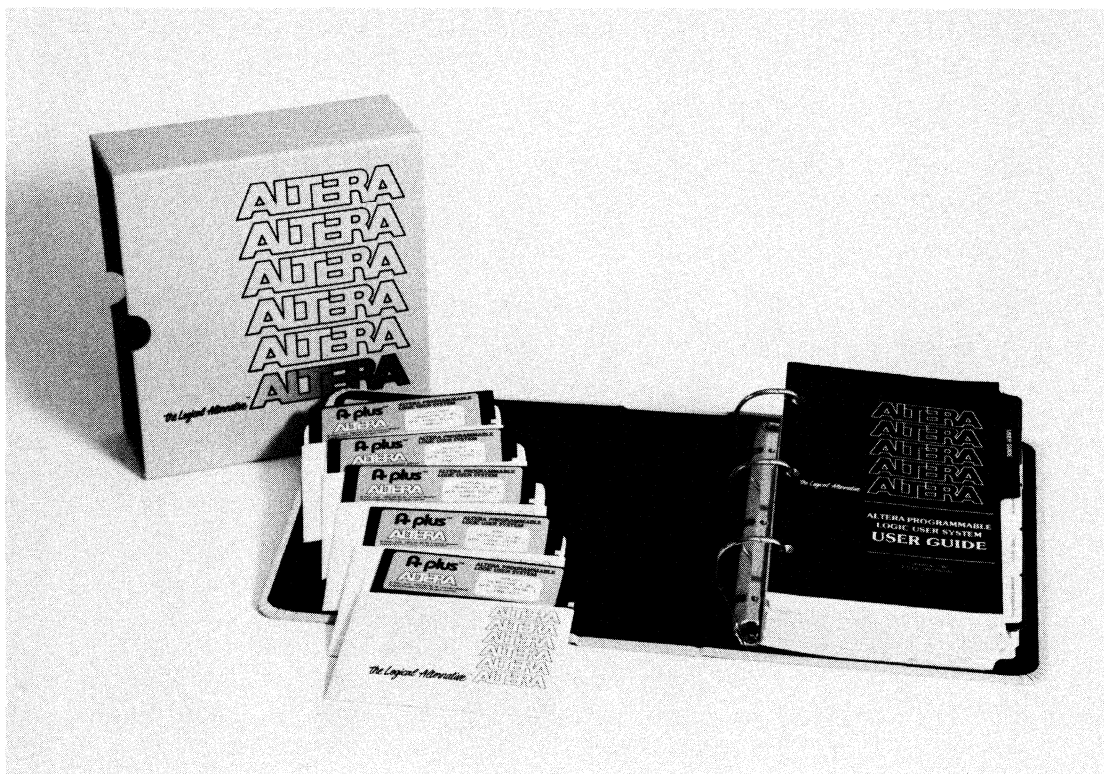
FEATURES

- Software support for all Altera General-Purpose EPLDs
- Software support for EPB1400 (BUSTER)
- Boolean Equation Design Entry
- MacroFunction design capability (with PLS4)
- Automatic pin assignments
- SALSA Logic Minimization
- Device fitter optimizes device resources
- Support for user-defined MacroFunctions
- Optional Schematic Design Entry interfaces
- Optional State Machine entry interfaces
- Optional Functional-Simulator interfaces
- PLS4 contains PLS2, LogiCaps and PLSLIB-TTL

GENERAL DESCRIPTION

A+PLUS, Altera Programmable logic user software, contained in the PLS2 and PLS4 products, is a series of software modules that transform a logic design into a programming file for Altera's general-purpose and function-specific EPLDs. A+PLUS supports a variety of input formats that may be used individually or combined together to meet the needs of a particular logic design task. These include Schematic Capture, State Machine, Boolean Equation, and Netlist Design Entry.

A+PLUS includes a Design Processor which transforms the input format to optimized code used to program the targeted EPLD. The Design Processor implements logic minimization , automatic EPLD part selection, architecture optimization, and design fitting. A+PLUS also includes LogicMap software for device programming.



REV. 3.0

FUNCTIONAL DESCRIPTION

Figure 2 shows the Block Diagram of the A+PLUS development software. A+PLUS accepts four different design entry formats: Schematic Capture, Netlist Capture, Boolean Equations, or State Machine input. The designer is not restricted to just one entry method but may 'mix-and-match' methods to best meet the needs of the overall logic design. If necessary, the design entry format is converted to an Altera Design File (ADF) which is the common entry format for the A+PLUS software. The ADF is then submitted to the Altera Design Processor (ADP). The ADP is composed of a set of modules integrated together that produce an industry standard JEDEC code used to program the EPLD. The Design Processor also produces documentation showing minimized logic and EPLD utilization. Once the JEDEC file is produced, the user may functionally simulate the design. Finally, the user can program the EPLD with the LogicMap programming software and Altera programming hardware or qualified third party programmers.

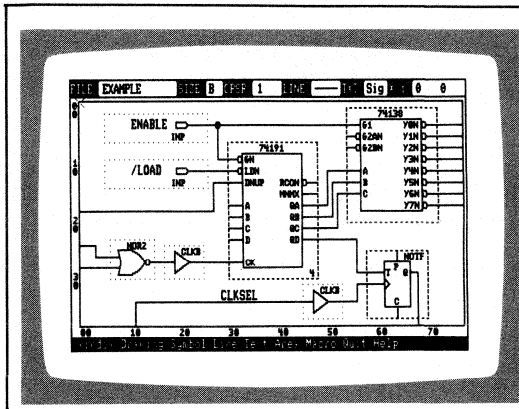
DESIGN ENTRY

SCHEMATIC CAPTURE (Included in PLS4)

Logic Designs may be entered from schematic drawings by using the LogiCaps or other schematic capture packages. Schematic capture design entry allows the user to quickly construct a wide range of logic circuits. Designs entered with this method use library primitives in the form of low-level functions (input, basic gates, flip-flops, and I/O primitives) to high level TTL MacroFunctions. LogiCaps is mouse-driven and supports hardcopy printout and plots. As required, the schematic representation is converted to an ADF file and processed by the A+PLUS software. For a more detailed description see the PLE40 LogiCaps data sheet.

LogiCaps is a high performance schematic capture package that has been optimized for entering designs destined for Altera EPLDs. It is the primary design entry platform for any member of the Altera EPLD family. When used in conjunction with TTL and user defined MacroFunction libraries, LogiCaps becomes the essential tool for the design of high density EPLDs.

The optional Altera design library is a collection of high level MSI building blocks which allow the LogiCaps user to enter designs in a "block manner".



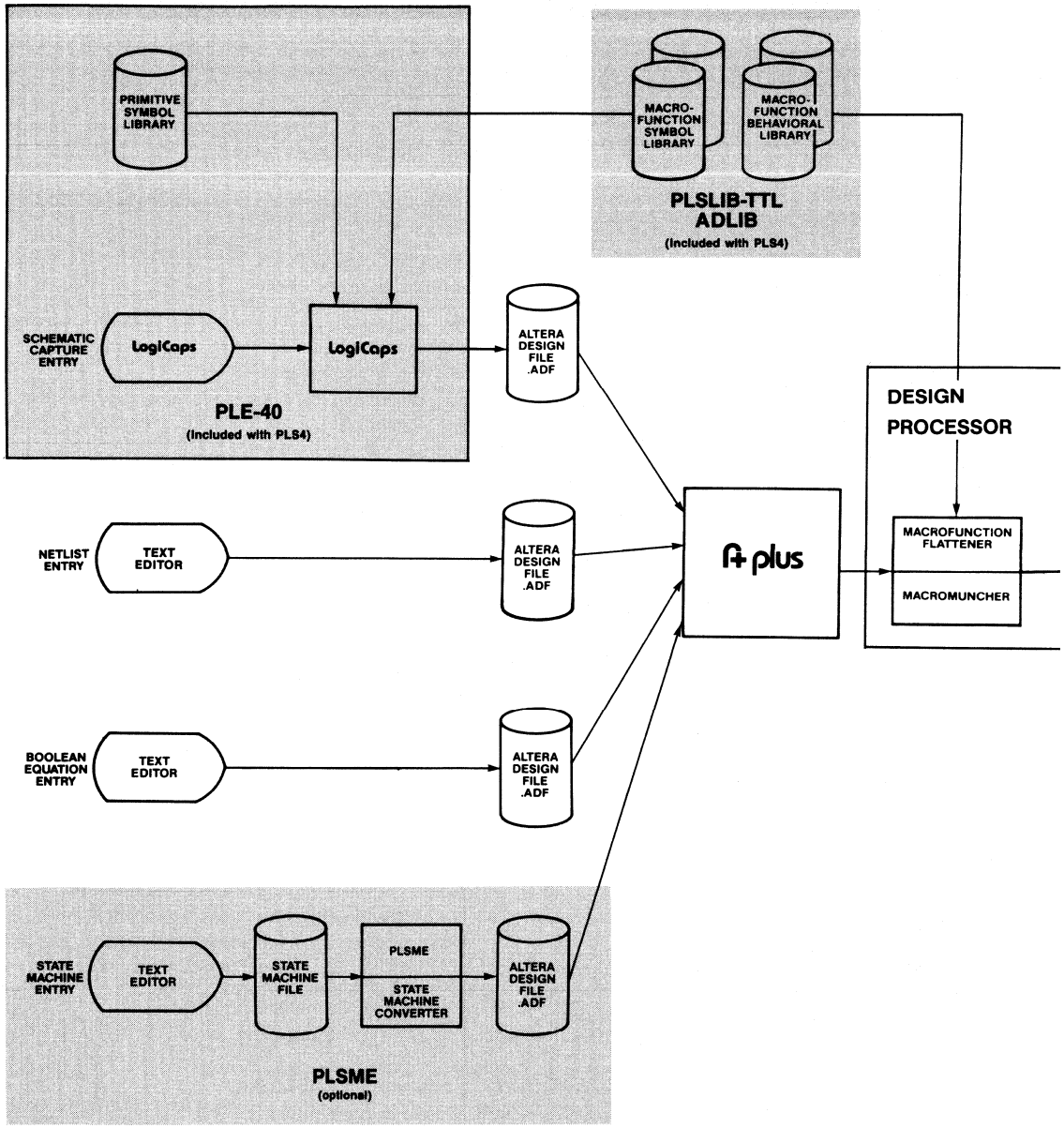
MacroFunction Libraries allow EPLD designs to be entered in LogiCaps using popular 7400 series symbols.

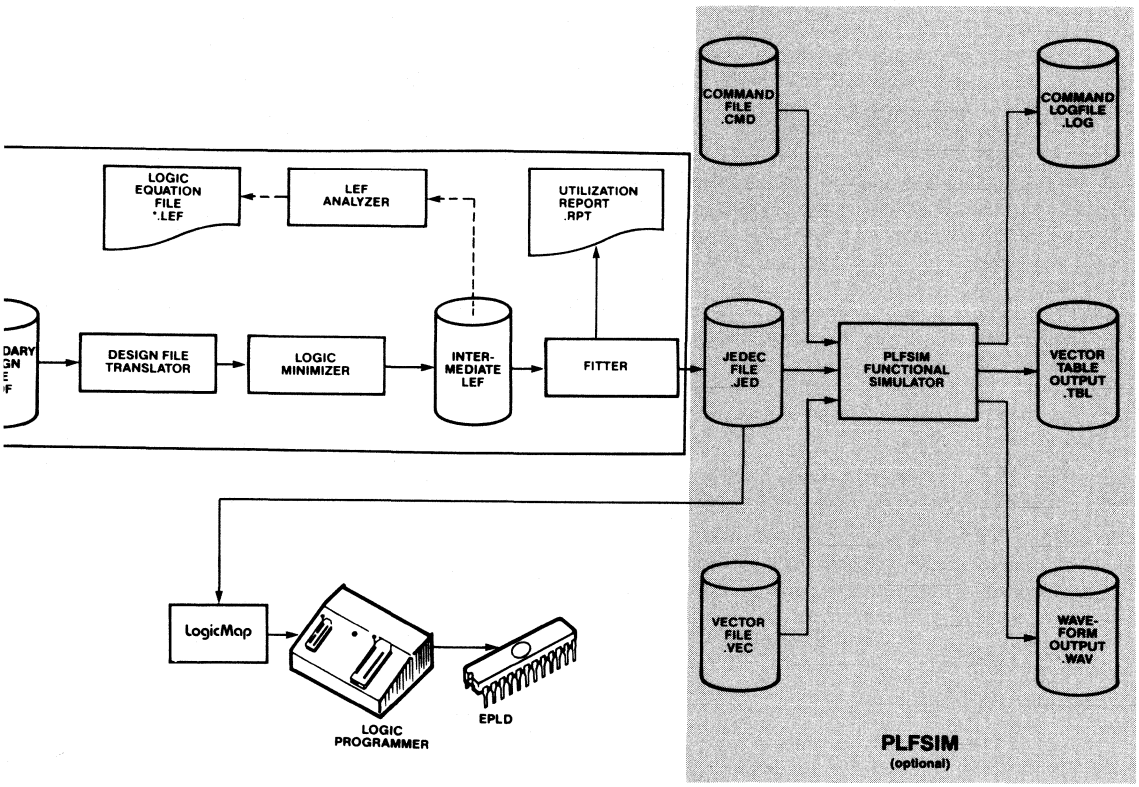
An initial primitive symbol library contains basic gate, flip-flop and I/O symbols as well as the most commonly used TTL SSI and MSI functions. Other design libraries include an extensive TTL 7400 series symbol library, and user-defined libraries. In addition, each library also contains logic functions not available in standard TTL or CMOS devices. Examples include counters implemented with toggle flip-flops, combination up/down counter with left/right shift register, and inhibit gates.

NETLIST ENTRY

The A+PLUS software directly supports netlist entry via the Altera Design File (ADF). Using a standard text editor, a netlist which describes the circuit is created by using a simple, high-level, design language. The netlist may contain basic gates, I/O architectures, boolean equations, and TTL MacroFunction descriptions. In addition, user defined comments and white space may be freely employed throughout the ADF file. The completed file is then submitted to the Design Processor. This entry method also permits circuit designers to utilize netlist outputs (e.g. from workstations or schematic capture packages not support by A+PLUS) that have been translated into ADF format.

FIG. 2 ALTERA EPLD DESIGN ENVIRONMENT




LOGIC EQUATION FILE *.LEF
LEF ANALYZER
UTILIZATION REPORT .RPT
DESIGN FILE TRANSLATOR
LOGIC MINIMIZER
INTER-MEDIATE LEF
FITTER
COMMAND FILE .CMD
JEDEC FILE .JED
VECTOR FILE .VEC
PLFSIM FUNCTIONAL SIMULATOR
COMMAND LOGFILE .LOG
VECTOR TABLE OUTPUT .TBL
WAVE-FORM OUTPUT .WAV
PLFSIM
(optional)
LogicMap
LOGIC PROGRAMMER
EPLD

BOOLEAN EQUATION

The Altera Design Processor compiles Boolean equation designs that are written in a simple design language. The source for the design may be created with any convenient text editor. The language supports free-form entry of all syntactical elements. Boolean equations need not be entered in sum-of-products form since the Design Processor will expand equations automatically. The multi-pass design processor/compiler has the ability to support intermediate equations. This feature permits significant reduction in the size of the Boolean equation source code and allow the designer to define the logic in the most natural conceptual manner.

STATE MACHINE (Optional)

Designs that are easily represented with state diagrams may be entered via the State Machine approach. This method uses a high-level language description featuring IF-THEN constructs, Case statements and Truth Tables. This design entry supports both Mealy and Moore state machines. Outputs of the state machine may be defined conditionally or unconditionally allowing flexible output structures that can be merged with other portions of the design. In addition, multiple state machines may be linked within the same design. Boolean equations are allowed offering the definition of high level intermediate logic expression. The software will also selects the optimum flipflops for the particular design. For more information on State Machine design entry see the PLSME data sheet.

DESIGN PROCESSOR

The Altera Design Processor (ADP) consists of a series of modules that translate design information from a variety of input sources into a JEDEC Standard File used to program the EPLD. This process is automatic and requires minimal assistance on the part of the circuit designer.

DESIGN FLATTENING

A+PLUS accepts design files from one or more of the design entry methods. Once the design has been submitted, the first function of the Altera Design Processor is to "flatten" the design from high-level MacroFunctions to low-level gate primitives. In order for designs to be flattened, information from the MacroFunction Behavioral Library is transferred to the design flattener, which in turn decomposes all MacroFunctions to their primitive gate equivalents.

MACROMUNCHING AND DEFAULT MODES

Once the design is flattened, the design processor analyzes the complete logic circuit and removes unused gates and flip-flops from any MacroFunction employed. This "MacroMuncher" allows the logic designer to freely employ high-level building blocks from the MacroFunction Symbol Libraries without the headaches of optimizing their use.

When MacroFunctions with unconnected inputs are detected, the design processor assigns "intelligent" default values. In general, active-high inputs default to GND and active-low inputs default to V_{CC} when left unconnected. This default mode is activated simply by leaving unused inputs without connections, thus eliminating "busy work" and enhancing productivity.

Once the design has been flattened, "munched", and all default values have been assigned, a secondary design file (SDF file) is produced for further processing

TRANSLATION/MINIMIZATION

The Translator takes the SDF file and checks for logical completeness and consistency. For example, the Translator validates that no two logic function outputs are shorted and that all logic nodes have an origin. In the event that the designer has chosen an EPLD name of "AUTO", the Translator will automatically select the appropriate EPLD based on the logic requirements of the design.

Logic minimization of designs is provided by the Minimizer module. Minimization phases include Boolean minimization with a SALSA (Speedy Altera Logic Simplifying Algorithm) that yields superior results to other heuristic reduction techniques. DeMorgan's theorem inversion can be applied automatically to equations. The processor contains algorithms based on artificial intelligence techniques to select candidate equations that will best be represented by a complemented AND/OR function. This feature significantly reduces product-term demands that can be generated by complex logic functions. For Altera EPLDs with selectable flip-flops, the Minimizer checks which type of flip-flop yields a more efficient solution and converts architecture if necessary. The minimized logic can then be optionally passed to the Analyzer module which converts the file into human-readable format allowing the designer to examine the minimized logic.

DESIGN FITTING

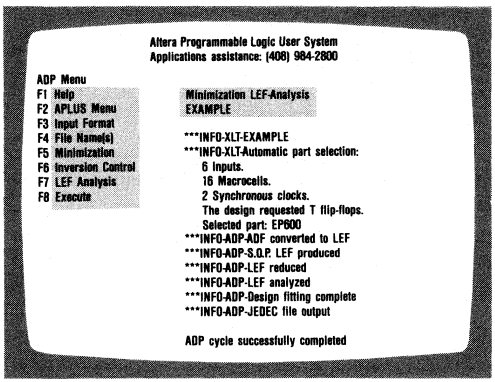
The fully minimized design is now transferred to the Fitter. This fitting routine relies on algorithms based on artificial intelligence software techniques in order to place and route the logic requirements of the design into the specified EPLD, automatically providing full pin assignments.

The Fitter module matches the requests of the design with the resources of the EPLD. The Fitter process encompasses all EPLD architectural attributes such as variable product term distribution, programmable flipflops, local and global busses and I/O requirements. If the designer specifies a pin assignment,

the Fitter matches the request. If no pin assignments are made, the Fitter finds an optimized fit for the design. The Fitter produces a Utilization Report that shows which of the EPLD's resources were consumed by the design and how. Finally, the Assembler module converts the fitted requests into an image for the part in a JEDEC Standard File.

FIG. 4 DESIGN PROCESSOR

The A+PLUS Design Processor displays status information during the compilation process. Complex design require only minutes to convert from design entry to programmed EPLDs.



LOGICMAP II

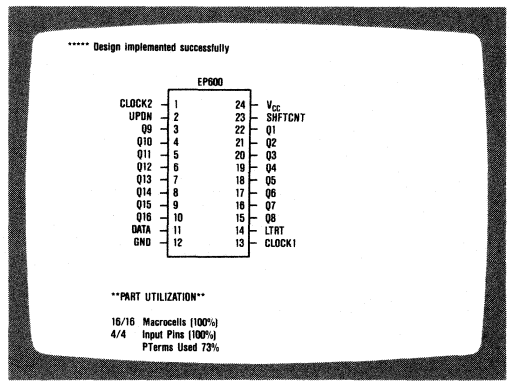
LogicMap II is the interface software that programs EPLDs from JEDEC files created by the Altera Design Processor. The program uses the Altera Super Adaptive Programming algorithm ASAP which significantly reduces device programming times. LogicMap II fully calibrates the programming environment and checks out the programming hardware when initiated. In addition, the program allows the designer to review the JEDEC object code generated by the Altera Design Processor in a structured manner. The program is fully menu driven and provides views of the device object code through a series of hierarchial windows. This feature permits low-level observation and editing of the design, viewed from a perspective similar to that of the logic diagram of the device in the datasheet. Individual EPROM bits within each Macrocell structure may be examined or changed if desired.

HARDWARE

LogicMap software is used to drive Altera programming hardware comprised of a software-configured programming card that occupies a single slot in the computer. Programming signals are transmitted to an external programming unit via a 30 inch ribbon cable and connector. The programming unit contains zero-insertion-force sockets for easy device insertion. All programming waveforms and voltages are derived by the Altera programming card so that no additional power sources are necessary. A programming indicator lamp on the programming unit is illuminated when the unit is active.

FIG. 5 UTILIZATION REPORT

The Utilization Report documents which of the EPLDs resources have been utilized. Shown below is a small portion of the report.



SYSTEM REQUIREMENTS

MINIMUM COMPUTER CONFIGURATION:

IBM XT and compatible machines
Monochrome display
640k bytes of main memory
10M byte hard disk drive and floppy drive
MS-DOS or PC-DOS versions 2.0 or later releases
Full-card slot for programming card

RECOMMENDED COMPUTER CONFIGURATION:

IBM AT and compatible machines
Color graphics or Enhanced graphics display (with extended memory)
640k bytes of main memory
20M byte hard disk drive and floppy-disk drive
MS-DOS or PC-DOS versions 3.2 or later releases
Full-card slot for programming card

LOGICAPS SCHEMATIC CAPTURE SOFTWARE

PLE40

PLE40 CONTENTS

SOFTWARE

- LogiCaps Schematic Capture.
- Printer/Plotter Interface.
- Standard Symbol Library

PLE40 FEATURES

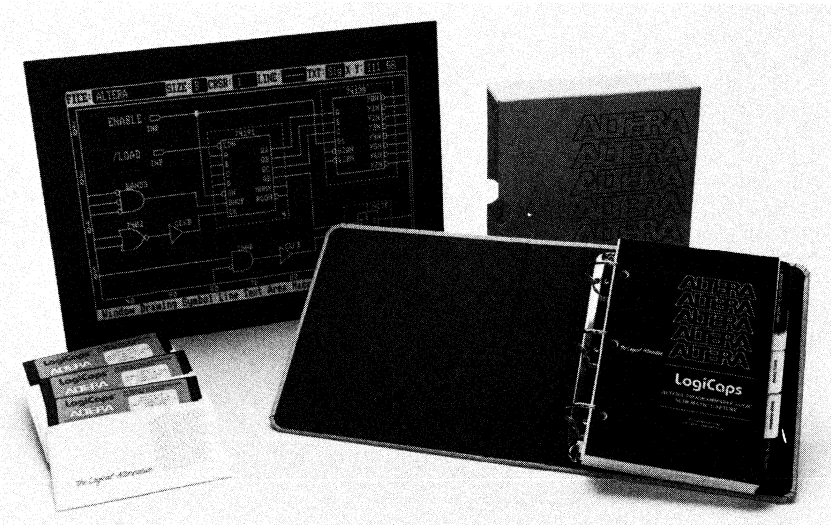
- Graphical Entry of Logic Schematics.
- Runs on IBM and compatible personal computers.
- Directly Interfaces with the Altera A+PLUS software system.
- Easy Mouse, Key, and Menu commands.
- Extensive on-line documentation.
- Dual window display mode.
- Multiple ZOOM levels.
- Orthogonal Rubberbanding of lines.
- Draw schematics up to 90" by 90".
- Tag and Drag editing.
- Area editing, save and load.
- User definable functions (MACROs).
- Schematic plotting with HP7475, 7580, and 7585 plotters.
- Support for CGA, EGA, or Hercules Graphics Cards.
- Standard Symbol Library contains 30 Macro-Functions and 80 MacroPrimitives.

GENERAL DESCRIPTION

Digital logic designs are often originally conceived in the form of a logic or schematic diagram. The engineer wishing to take advantage of the many benefits of the new high density programmable logic devices should not need to convert those designs to arcane Boolean logic equations simply to please the computer. Ideally the engineer should be able to directly enter the design in the original schematic form, then allow software to extract the equations. LogiCaps fulfills this task by allowing the user to literally draw the schematic on a computer screen. Additional benefits are realized by the electronic medium, such as the ease of editing designs.

ORDER INFORMATION

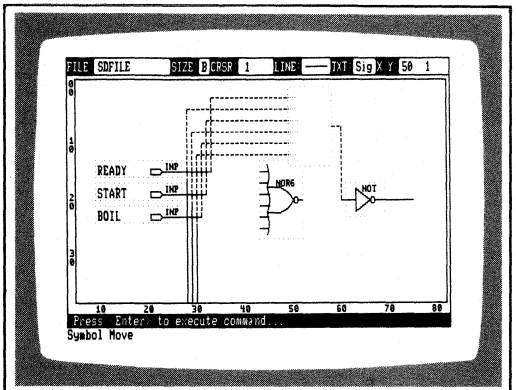
PLE40



REV. 2.0

FUNCTIONAL DESCRIPTION

LogiCaps is a fast, powerful, yet inexpensive schematic capture system that has been optimized for entering designs destined for Altera programmable logic devices. Schematic diagrams are drawn on the screen of a personal computer using a mouse; then, with a single command, a netlist file is generated ready to be programmed into silicon. LogiCaps complements the Altera Programmable Logic User System (A+PLUS), forming a complete interactive EPLD development system. An engineer could start with a blank "sheet" on a PC, then in minutes transform a circuit idea into a working, user configured integrated circuit.



Rubberbanding lines while moving symbols or areas makes editing an easy task.

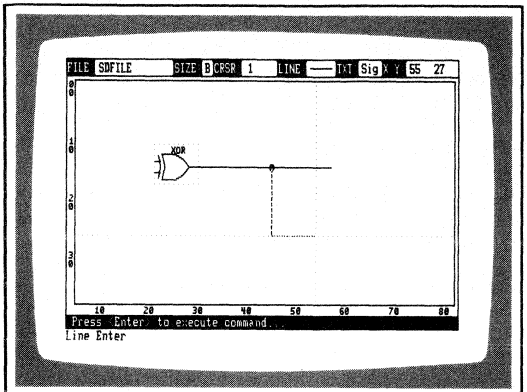
The most frequently used functions—drawing and connecting lines, moving and copying objects, and just getting around in the drawing—are done by simple mouse motion or pressing a mouse button. Functions used less often are executed by pressing a single key, while those functions rarely used or requiring more data are selected from a nested command menu system. No command requires more than three key presses to execute, unless a file name or some other text is needed.

Commands follow a simple, intuitive format that eliminates the initial learning curve normally associated with software this powerful. Menus or prompts are always present telling you what to do next, and extensive on-line help information is available for every menu.

LogiCaps was designed with the WYSIWYG philosophy: What-You-See-Is-What-You-Get. There are no underlying data structure "surprises". The internal data structure is fully represented by the visible drawing. LogiCaps is so obvious in use, that you could easily become a proficient user within minutes of your first session!

Orthogonal rubberbanding means you may move symbols and areas of the drawing about and let the software worry about keeping the lines connected.

Mouse functions are context driven: if you press a



Line drawing on LogiCaps.

button with the cursor in a symbol, you probably want to do something with that symbol. If the cursor is on a line or on some text, you likely wish to move or copy that line or text. Otherwise perhaps you wish to draw a new line, move or copy an area, or make an interconnection dot. All of these things may be done using the mouse, and the selection happens in a natural, intuitive manner.

There are 5 line types and 4 character sets, providing flexibility in schematic drawings. Drawing size may be set for the standard A,B,C,D, or E sizes. Complex symbol shapes are stored as library files for compactness and maximum flexibility. Areas of drawings may be saved to and loaded from drawing files, allowing the user to build a library of standard modules that may later be combined in other applications. All of the function keys, in addition to having their pre-assigned functions, may be programmed to execute a user defined sequence of keystrokes (and/or mouse functions). These sequences may be as simple as executing one function, or as complex as entering a 2000 gate design complete with documentation and generating the ADF file.

The screen refresh rate of LogiCaps is faster than any other equivalent schematic capture system on the market. This makes for a highly responsive and productive software tool. In addition, many features are provided to make the drawing entry task as quick as possible. These features include a dual window capability, permitting the user to view two independent regions of the drawing at once and jumping between them at the press of a key. The dual window capability also allows you to have simultaneous views at different zoom levels: you can see both the trees AND the woods! Other features include quick jumps to previously saved locations, a sophisticated reference grid system for easy alignment of objects in the drawing, and special cursor key modes including panning across the drawing.

MAJOR FEATURES OF LOGICAPS

DRAW SCHEMATICS UP TO 90" BY 90"

Drawing size may be set to the standard A,B,C,D, or E sizes, plus the maximum size of 90" by 90". Objects are positioned on a .10" grid, providing 10 units per inch. Cursor coordinates are displayed as well as reference indices, so you always know your location within the drawing.

OUTPUTS ALTERA DESIGN FILE

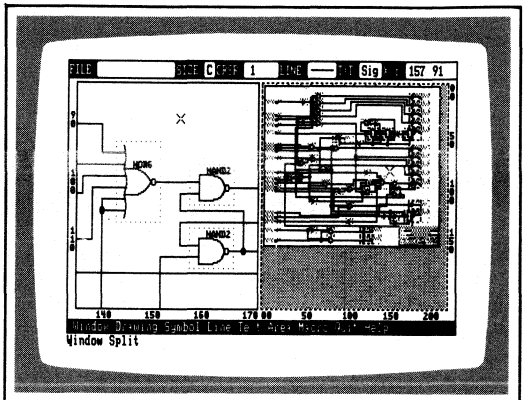
LogiCaps produces an Altera Design File (ADF) netlist directly from the schematic drawing. No intermediate programs need to be executed; thus EPLD designs can be iterated without leaving the A+PLUS design environment.

EASY MOUSE, KEY, AND MENU COMMANDS

Sixty-two commands are arranged in a nested command menu structure for easy, consistent selection. Function and cursor keys and mouse commands add efficiency and speed to the Engineer/LogiCaps interface.

SELECTABLE DUAL WINDOW MODE

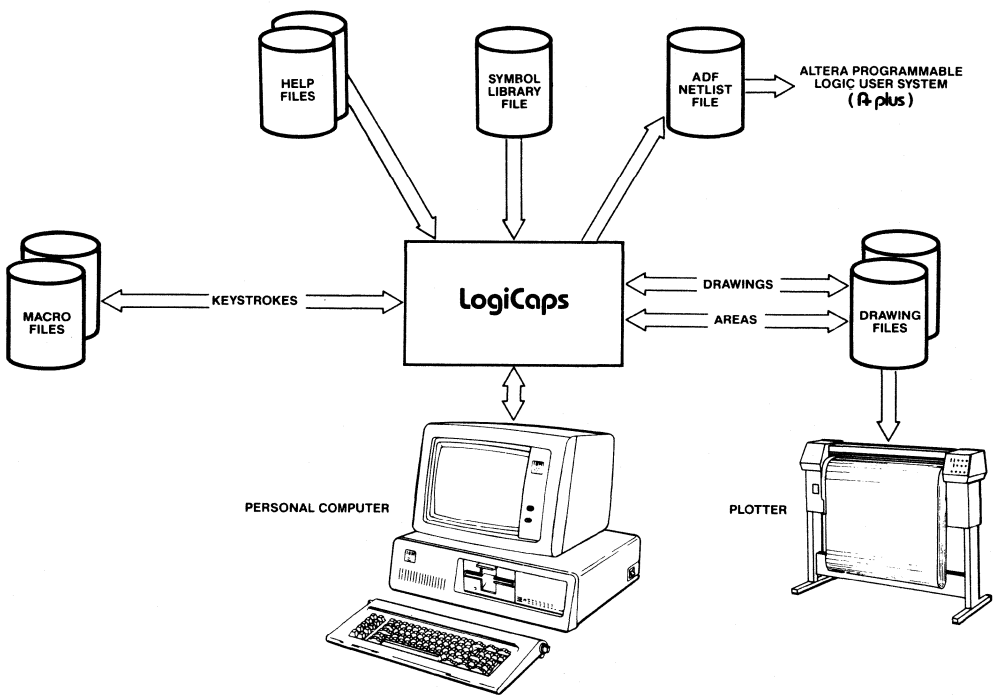
Allows the designer to see the overall schematic and yet be able to work in detail on part of the design without needing to ZOOM in and out, or to view two different parts of the design and quickly jump back and forth between them.



Dual windows allows you to see the trees AND the forest at the same time.

MULTIPLE ZOOM LEVELS

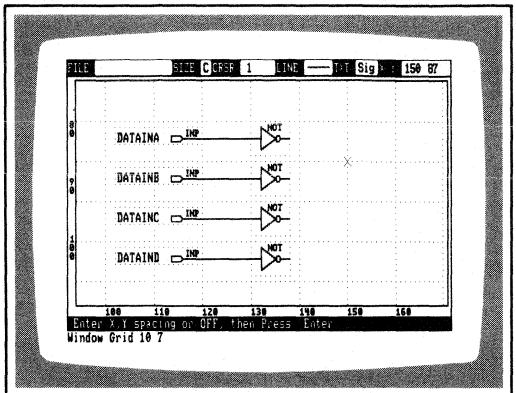
Single keystroke commands allow an immediate change of perspective of the design. ZOOM-IN for detail; ZOOM-OUT for an overview. Multi-levels provide useful intermediate views that can be used for wider regional editing.



LogiCaps reads and writes drawing files, macro files, symbol library files, Help files and ADF files.

ORTHOGONAL RUBBERBANDING

LogiCaps features true orthogonal rubberbanding. This means that symbols and areas can be moved, and yet the connection wires retain 90-degree angles as they move to maintain the connectivity of the schematic. This enables the designer to "clean up" a design and make first-class drafting quality schematics.



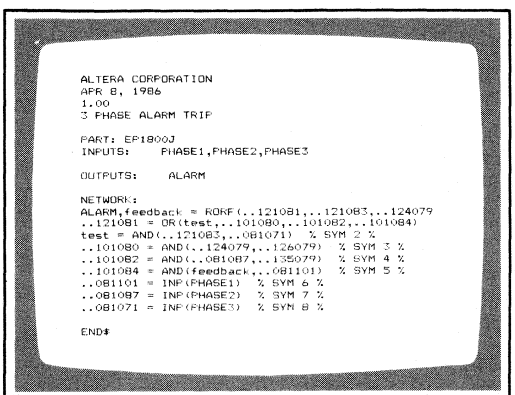
Reference grid system is used to align objects.

ALTERA PRIMITIVE SYMBOL LIBRARY

Over 80 logic and I/O symbols provide the basic building blocks for logic schematics. Familiar names like "AND2" and "XOR" identify the logic symbols, and mnemonic symbols like "RORF" (Register Output, Register Feedback) define the EPLD I/O architecture configurations. See figure on page 6.

USER DEFINABLE MACROS

Frequently used command sequences can be saved by the user as macro recordings. These recordings may then be executed by a single keypress. This speeds design entry and allows customization of LogiCaps to suit the designer's own preferences.



```
ALTERA CORPORATION
APR 8, 1986
1.00
3 PHASE ALARM TRIP

PART: EP1800J
INPUTS:     PHASE1,PHASE2,PHASE3

OUTPUTS:    ALARM

NETWORK:
ALARM,feedback = RORF(..121081,..121083,..124079
..121081 = OR(test,..101080,..101082,..101084)
test = AND(..121083,..081071)   % SYM 2 %
..101080 = AND(..124079,..126079)   % SYM 3 %
..101082 = AND(..081087,..135079)   % SYM 4 %
..101084 = AND(feedback,..081101)   % SYM 5 %
..081101 = INP(PHASE1)   % SYM 6 %
..081087 = INP(PHASE2)   % SYM 7 %
..081071 = INP(PHASE3)   % SYM 8 %

END$
```

The Altera Design File (ADF) netlist is directly generated by LogiCaps, ready for processing by A+PLUS.

TAG AND DRAG EDITING

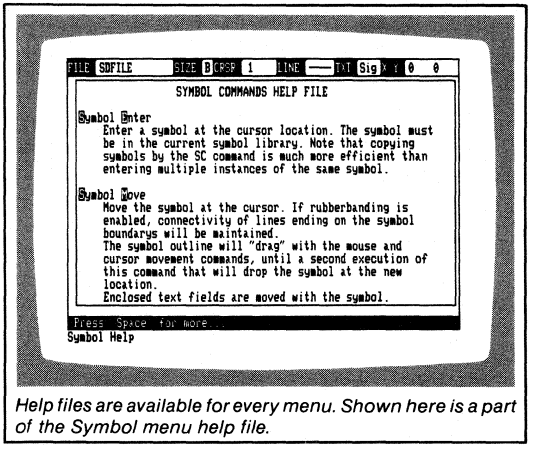
To move an object to a new position is as simple as positioning the cursor on the object and pressing a button. An outline of the object can then be moved to the new location where another press of a button will move the object there. A different button can be used for making copies of the object if that is desired.

AREA EDITING FUNCTIONS

Whole areas of a schematic can be moved, copied, erased, saved, or loaded. This makes construction of repetitive sections of a design a snap. Through this technique a designer can build up his own library of sub-circuit functions that may be used in many different EPLD designs.

"WHAT YOU SEE IS WHAT YOU GET" DESIGN PHILOSOPHY

LogiCaps derives the netlist directly from the graphical drawing database. There are no hidden connections or broken nets that appear to be connected.



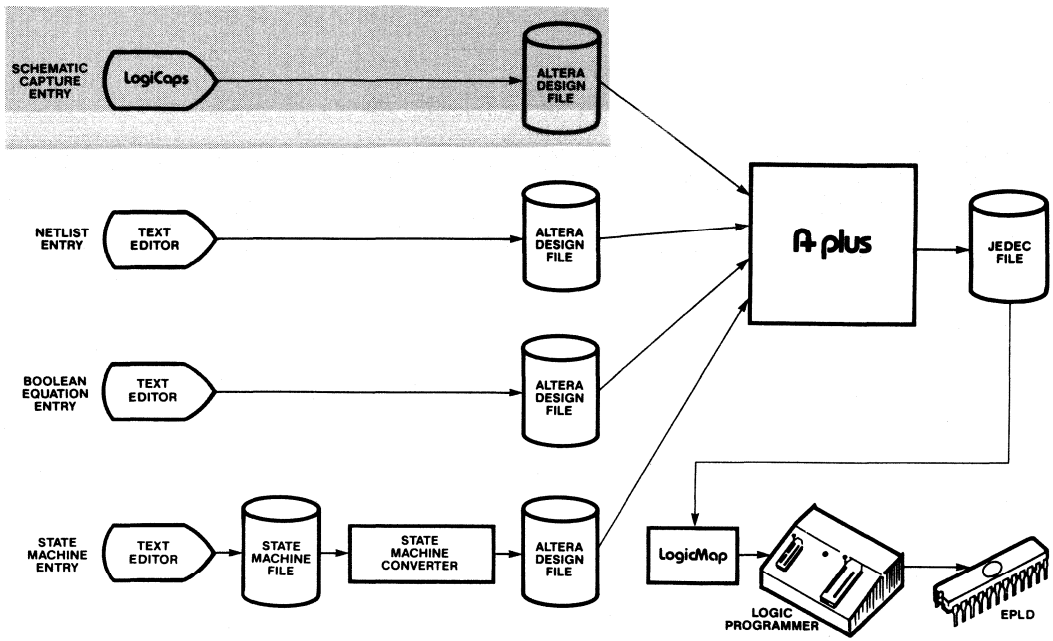
Help files are available for every menu. Shown here is a part of the Symbol menu help file.

EXTENSIVE ON-LINE DOCUMENTATION

Every menu includes a HELP function with explanation of all selections available in that menu. The primary menu HELP text also explains key functions and other aspects of the system.

DRAWING SIZES/REFERENCE LETTERS

Size	inches	millimeters
A	8½ × 11	216 × 279
B	17 × 11	432 × 279
C	22 × 17	558 × 432
D	34 × 22	864 × 558
E	44 × 34	1118 × 864
F	90 × 90	2286 × 2286



LogiCaps operates in conjunction with, and is a natural enhancement to, the Altera Programmable Logic User System (A+PLUS). It provides a complete path from the engineer's design concept to a programmed EPLD.

Window	Drawing	Symbol	Line	Text	Area	Macro	Quit	Help
MoveXY	Load	Enter	Enter	Enter	Boundary	Record		
Pan	Write	Move	Move	Move	Move	Play		
Tag	Delete	Copy	Copy	Copy	Copy	Stop		
Recall	Size	Delete	Delete	Delete	Delete	Assign		
Zoomset	Files	Reflect	Join	Select	Toggle	Clear		
Split	ADF	List	Select	Find	Load	Files		
Grid	Help	Find	Bend	Import	Write	Help		
Auto		Numbers	Rubberband	Borders	Files			
Color		Help	Help	Help	Help			
Help								

LogiCaps Main Command Menu (across the top) and sub-menus (columns under selections). All selections are made by a single keypress (first letter of name) and each menu includes a HELP selection.

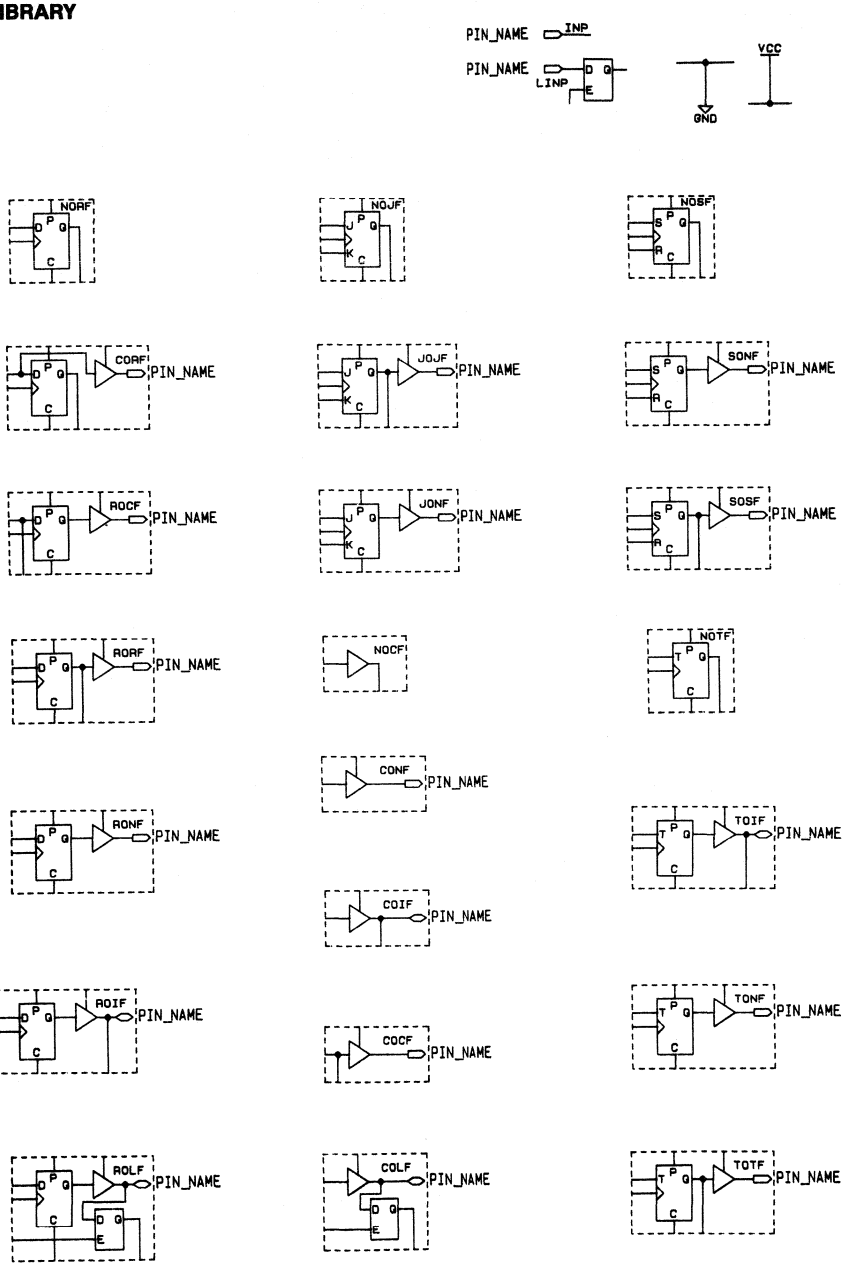
MOUSE MANUFACTURERS

LOGITECH, Inc.
805 Veterans Blvd.
Redwood City, CA 94301
(415) 365-9852

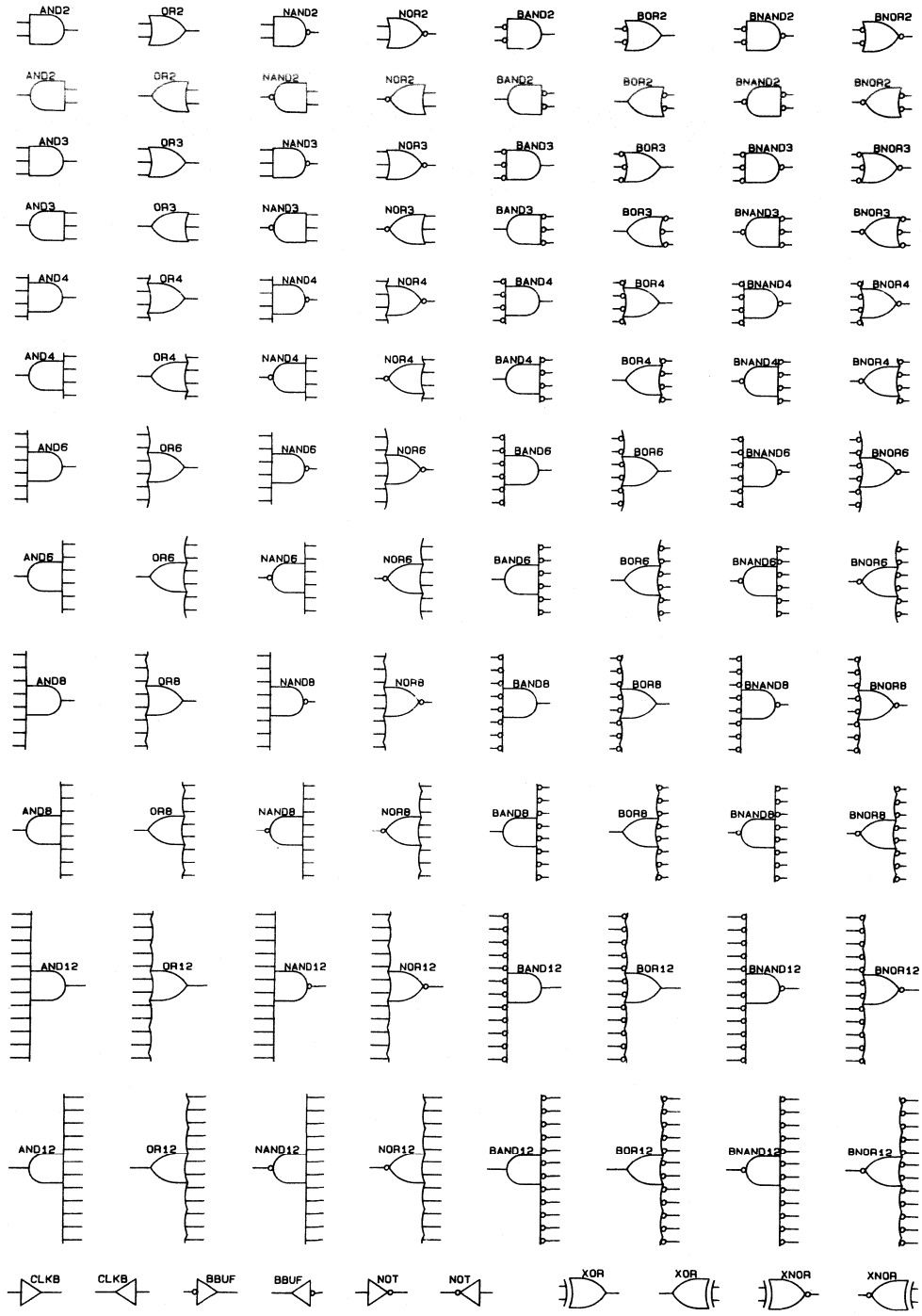
MOUSE SYSTEMS Corp.
2336H Walsh Ave.
Santa Clara, CA 95051
(408) 988-0211

LogiCaps

SYMBOL LIBRARY



The LogiCaps symbol library provides the building blocks for logic design. The drawing shown here is an example of LogiCaps plotter output.


AND2
OR2
NAND2
NOR2
BAND2
BOR2
BNAND2
BNOR2
AND2
OR2
NAND2
NOR2
BAND2
BOR2
BNAND2
BNOR2
AND3
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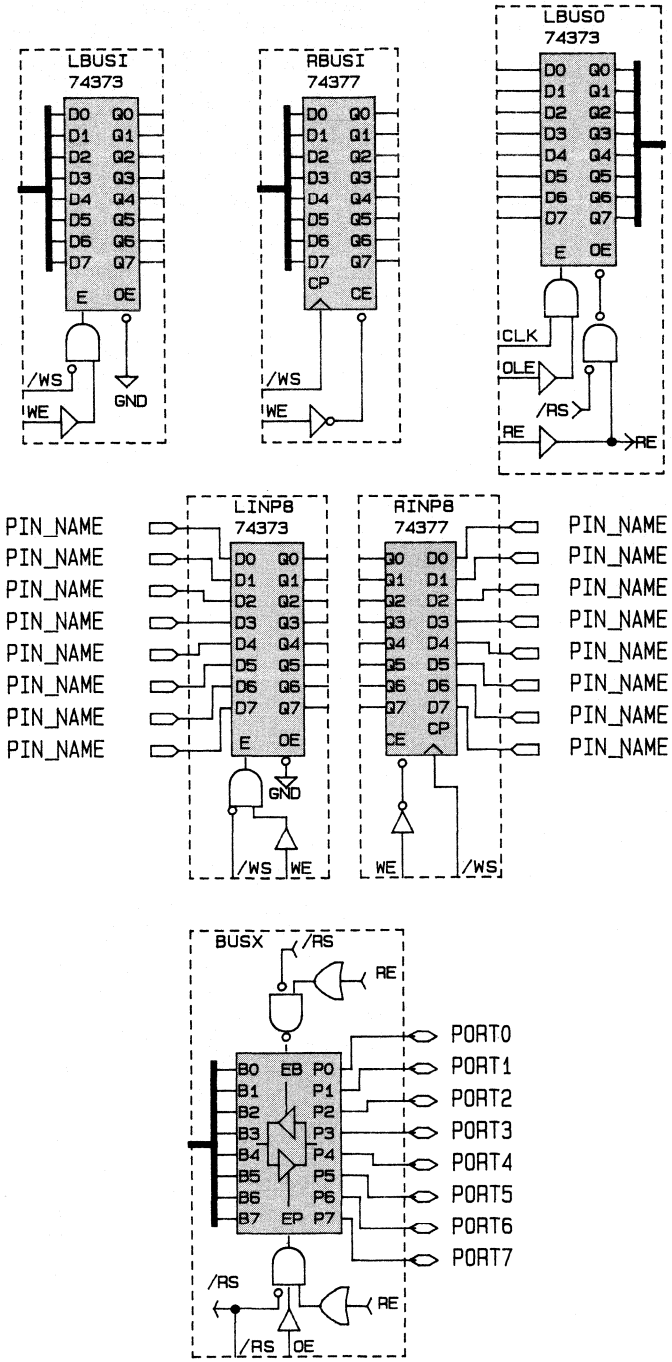
BOR12
BNAND12
BNOR12
AND12
OR12
NAND12
NOR12
BAND12
BOR12
BNAND12
BNOR12
CLKB
CLKB
BBUF
BBUF
NOT
NOT
XOR
XOR
XNOR
XNOR

BUSTER PRIMITIVES



TTL MACROFUNCTION LIBRARY PLSLIB-TTL

PLSLIB-TTL CONTENTS

- TTL MacroFunction Library Diskette
- ADLIB, Altera Design Librarian Diskette.
- TTL MacroFunction User Manual.

PLSLIB-TTL FEATURES

- 100+ Different MacroFunctions.
- Allows High Level Design Entry.
- Used With LogiCaps Schematic Entry.
- User Definable Symbols and MacroFunctions with ADLIB.
- MacroMunching of Unused Gates.
- Increase Design Productivity.
- Supported by A+PLUS Version 4.5 or Later.

ORDER INFORMATION

PLSLIB-TTL

GENERAL DESCRIPTION

To increase design ease and productivity Altera has created MacroFunctions. These are high level building blocks that allow the user to design at the TTL level. This ability aids a first-time user since the TTL functions will already be familiar. The experienced EPLD user will also benefit by being able to increase design productivity with the use of MSI function blocks.

Most MacroFunctions are commonly used 7400 series SSI and MSI TTL parts. A few are specific to Altera and are particularly well suited for logic design with Altera EPLD architecture. These have been designed by EPLD design experts and contain inner logic behavior to maximize EPLD speed and utilization.

Altera MacroFunctions are very versatile. They can be used together with user designed Macro-Functions and/or with Altera low level logic primitives depending on the logic needed. The inputs and outputs of the EPLD to be programmed are specified with Altera I/O design primitives.

REV. 2.0

MACROFUNCTION LIBRARY

The PLSLIB-TTL library contains over 100 functions. This library includes the most commonly used TTL parts such as counters, decoders, encoders, shift registers, flip-flops, latches, multipliers, etc. The parts in the library were carefully chosen so that any TTL function not already in the library can be easily implemented using an existing part and some Altera low level gate primitives. The Table below shows the presently available MacroFunctions.

MACRO-MUNCHING

A unique function built into the A+PLUS Design Processor ensures that the use of MacroFunctions causes no loss of design efficiency. The A+PLUS Design Processor analyzes the complete logic circuit and automatically removes unused gates and flip-flops from any MacroFunction used. This Macro-Muncher allows the user the ease of designing at the TTL level with the efficiency of gate level design. It also alleviates the headaches associated with optimizing the use of TTL parts.

In Figure 2, the MacroFunction will use up to 8 Macrocells if all of the inputs and outputs are connected. For this application only half of the outputs are desired so only half of the Macrocells are needed. When this MacroFunction is put through the A+PLUS Design Processor it will only use 4 Macrocells.

USING MACROFUNCTIONS

The following example shows the ease of designing with MacroFunctions and the efficiency of using EPLDS. In this example, it is desired to design a chip that will act as a BCD counter that gives the user the ability to choose 1 of 4 different counting speeds and have the outputs drive a seven-segment LED display. The basic strategy for the design is shown in Figure 3.

By looking at the Table of available MacroFunctions it is seen that the 7446 is a suitable seven-segment decoder, the 74162 is a BCD counter, the 74153 is a 4-to-1 multiplexer, and that FREQDIV is an Altera-provided frequency divider. So, everything needed in the design is already available in the MacroFunction Library.

To design the chip, the desired inputs and outputs are wired to Altera I/O design primitives and the MacroFunctions are wired together just as the actual TTL chips would be wired. The actual design is shown in Figure 4. The output primitive Y1 is connected to the output of the multiplexer to keep the number of P-terms under 8. Notice that the unused inputs and outputs of the MacroFunctions were left unconnected and how this helps alleviate design clutter.

Like all designs containing MacroFunctions, the Macro-Muncher takes a bite out of this design by eating the unused part of the 74153 and the rest of the unused logic in the design. Also notice the ease of inverting the CLEAR input to the 74162 MacroFunction. This would require another whole chip if the design was being done with individual chips.

This entire design containing 5 TTL functions is implemented in an EP600 using the A+PLUS 4.5 Design Processor. Hence, the entire design is completed. It takes less time than it would take to wire the individual chips together, and it comes in one package which eliminates the chances of wiring mistakes.

On the following pages are the MacroFunctions that are presently available. They are compatible with the LogiCaps schematic capture package and are supported by A+PLUS.

TABLE OF AVAILABLE MACROFUNCTIONS

TYPE	AVAILABLE
Adders	7480, 7482, 7483, 74183, 8FADD
Comparators	7485, 74158, 8MCOMP, 74518
Converters	74184, 74185
Counters	7493, 74160, 74161, 74162, 74163, 74190, 74191, 74160T, 74161T, 74162T, 74163T, 74190T, 74191T, 74192T, 74193T,
	74393, 8COUNT, 4COUNT, 16CUDSLR, UNICNT2, GRAY4
Decoders	7442, 7443, 7444, 7445, 7446, 7447, 7448, 7449, 74138, 74139, 74154, 7155, 74156
Flip-Flops	7470, 7471, 7472, 7473, 7474, 7476, 7478, 74173, 74174, 74175, 74273, 74374
Freq Divider	FREQDIV
Latches	7475, 7477, 74116, 74259, 74279, 74373, NANDLTCH, NORLTCH
Multipliers	74261, MULT2, MULT24, MULT4
Multiplexers	74147, 74148, 74151, 74153, 74157, 74158, 74298, 21MUX
Parity Generators	74180, 74280
Shift Registers	7491, 7494, 7496, 7499, 74164, 74165, 74166, 74178, 74179, 74194, 74198, 16CUDSLR, BARRELST, UNICNT2
SSI Functions	7400, 7402, 7404, 7408, 7410, 7411, 7420, 7421, 7427, 7430, 7432, 7486, INHB, CBUF
Storage Registers	7498, 74278
True/Comp Elements	7487
ALU	74181

USER DEFINED MACROFUNCTIONS

In addition to provided TTL elements, users may create their own MacroFunctions using ADLIB (Altera Design Librarian). ADLIB takes the custom logic functions described with basic gates, flip-flops, boolean equations and TTL symbols and automatically generates a MacroFunction symbol and behavioral description to be used with LogiCaps and A+PLUS. Users may define signal position and input default values within this newly created symbol. ADLIB is a powerful tool for creating customized MacroFunctions or hierarchical designs with many nested levels.

FIG. 2

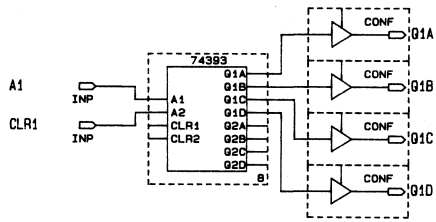


FIG. 3

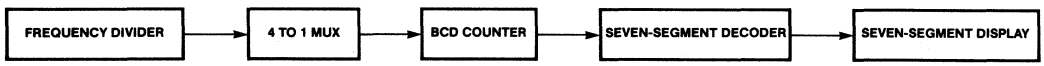
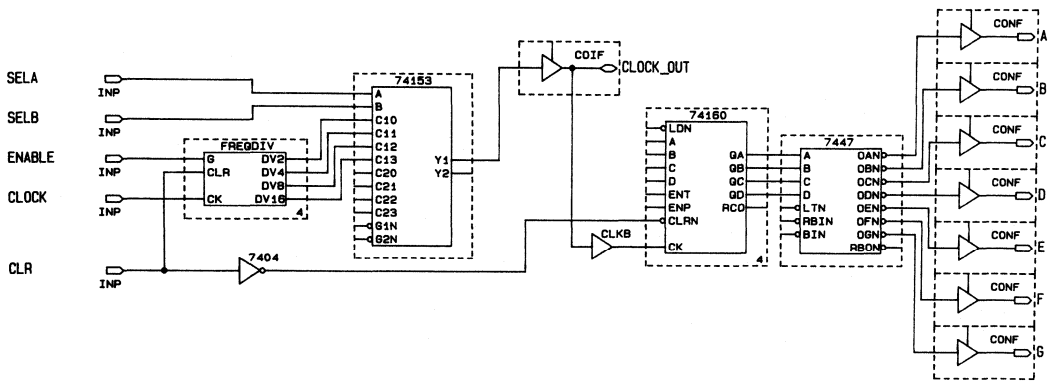
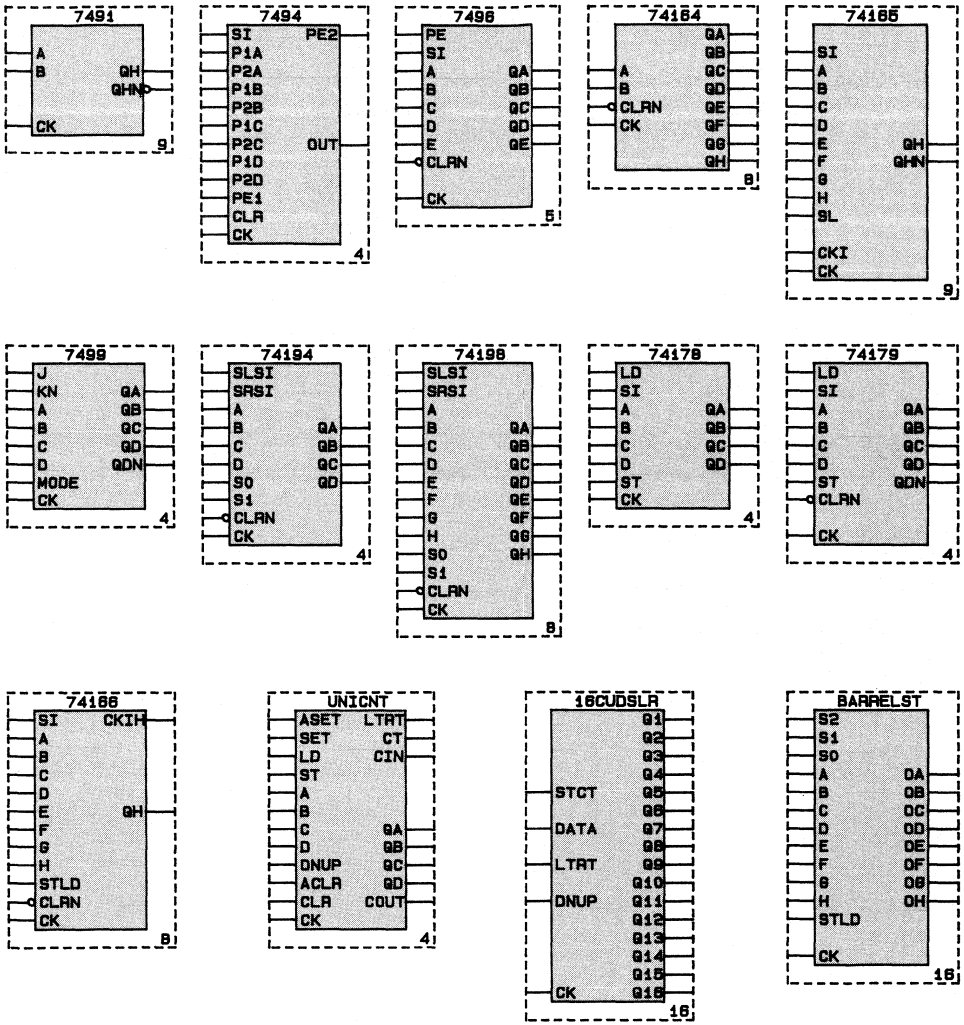


FIG. 4

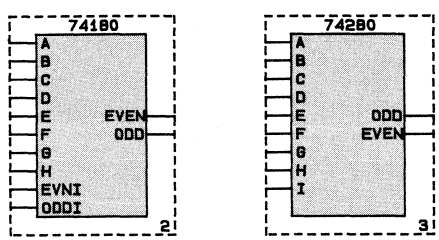


MACROFUNCTION LIBRARY

SHIFT REGISTERS

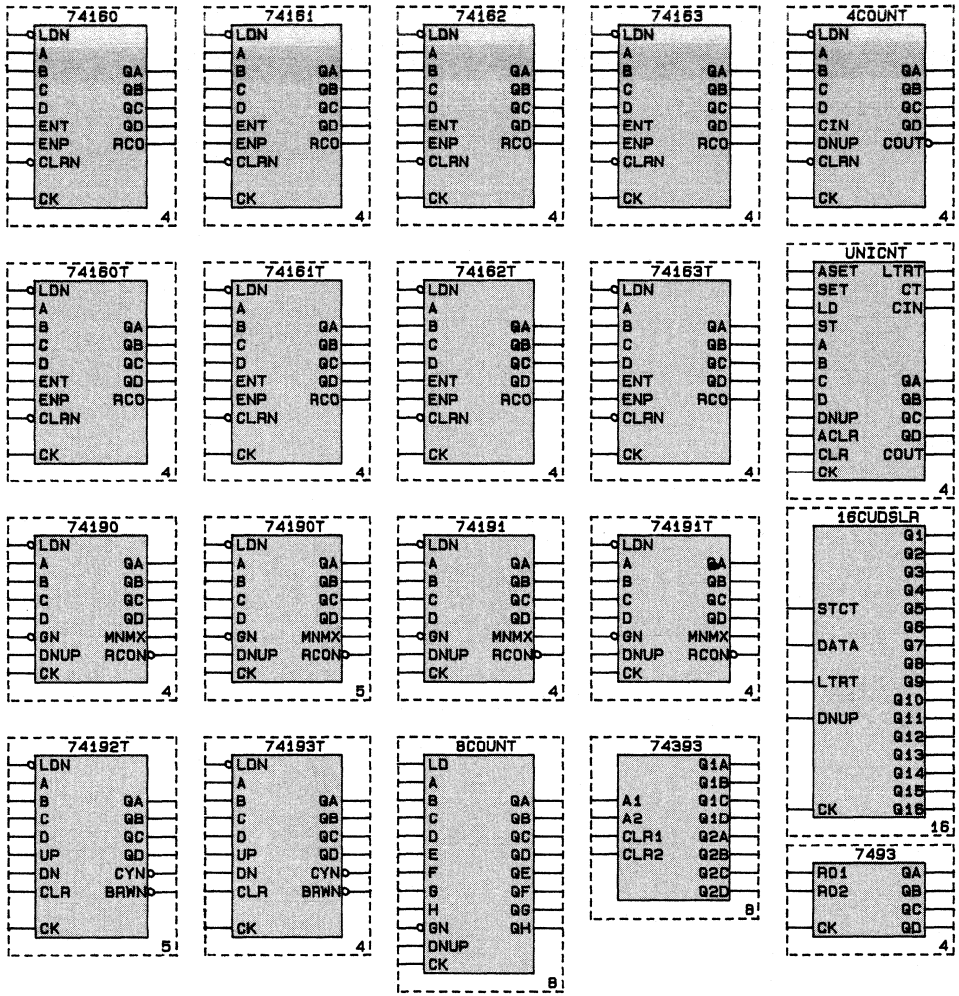


PARITY GENERATORS

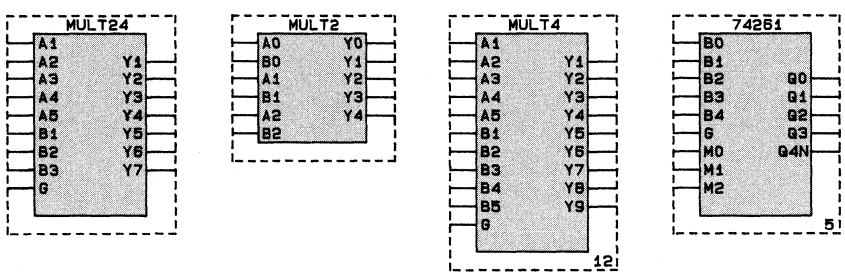


MACROFUNCTION LIBRARY

COUNTERS



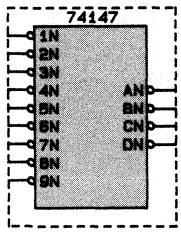
MULTIPLIERS

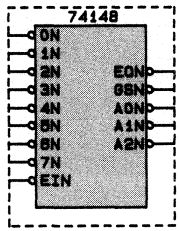


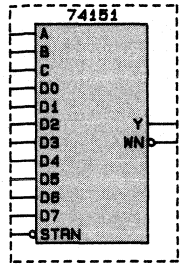
ALTERA

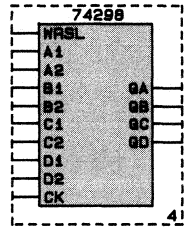
MACROFUNCTION LIBRARY

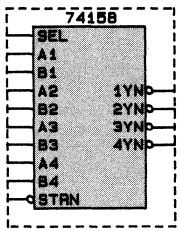
MUX/ENCODERS

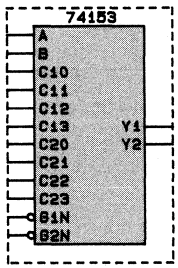


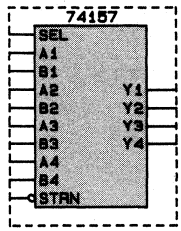


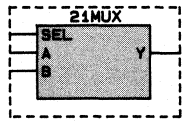




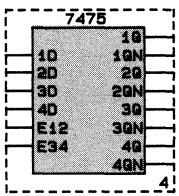


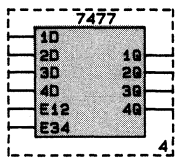


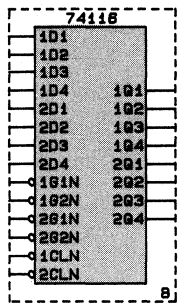


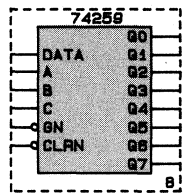


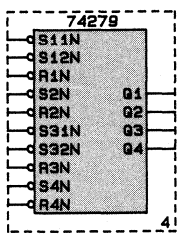
LATCHES

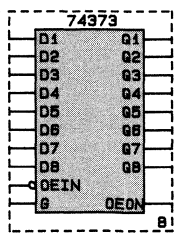


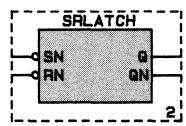






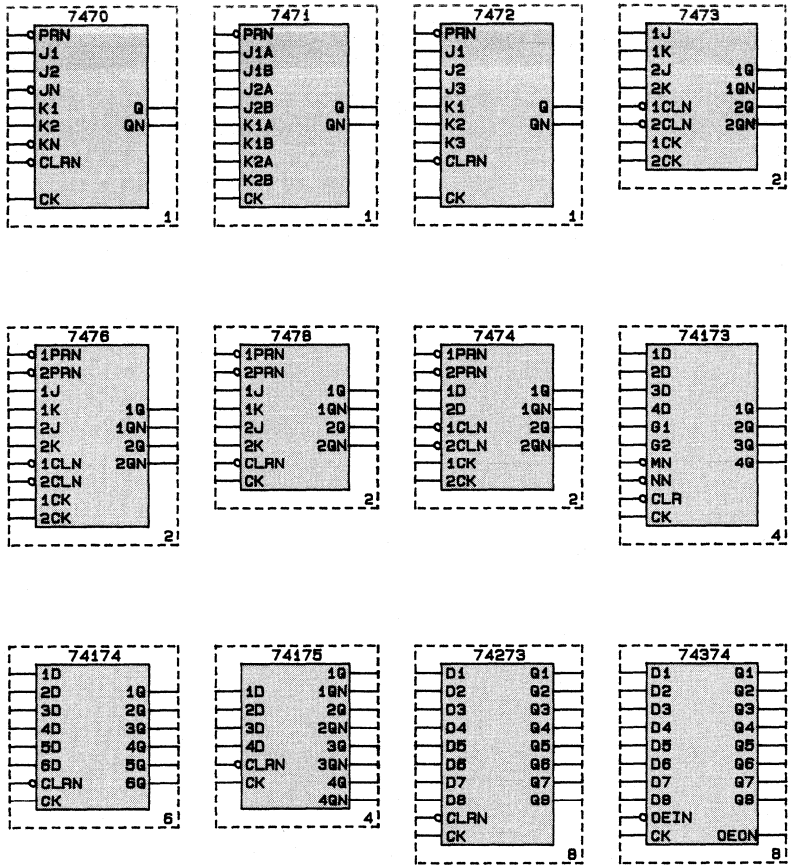




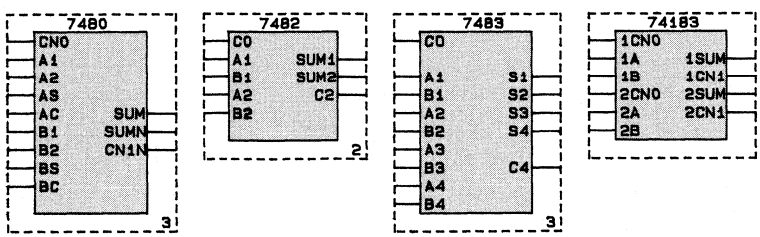


MACROFUNCTION LIBRARY

FLIP-FLOPS/REGISTERS



ADDERS



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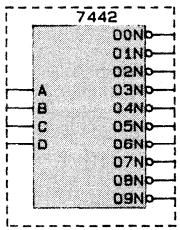

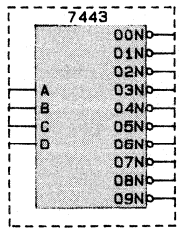

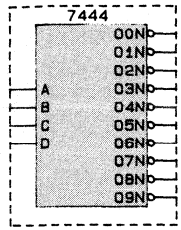

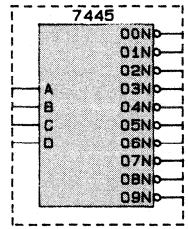

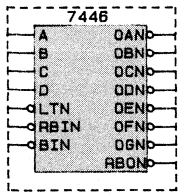

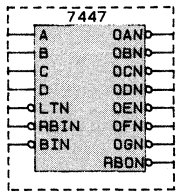

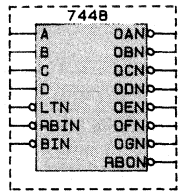

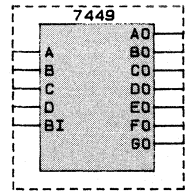

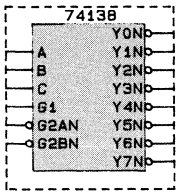

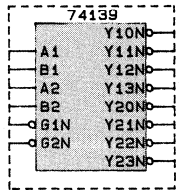

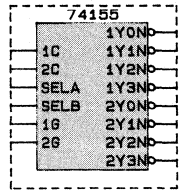

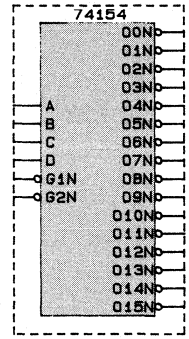

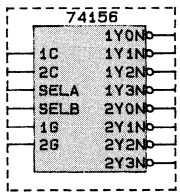

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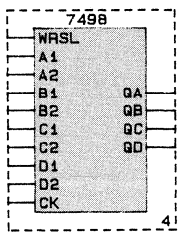
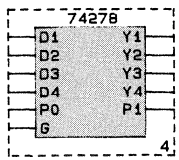
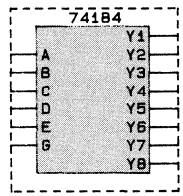
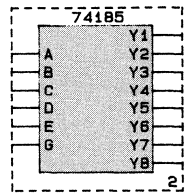




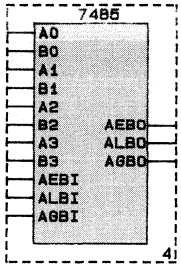
CONVERTERS

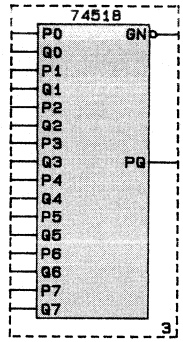


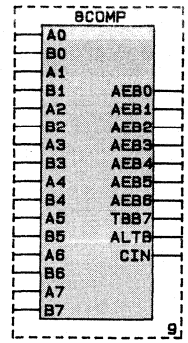


MACROFUNCTION LIBRARY

COMPARATORS







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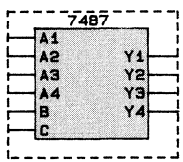
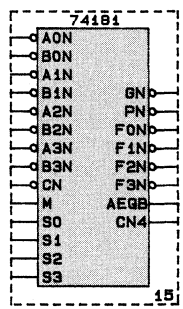
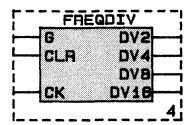


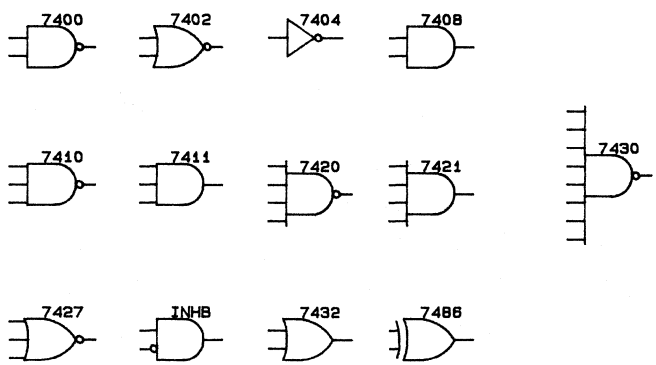
ALU



FREQUENCY DIVIDER

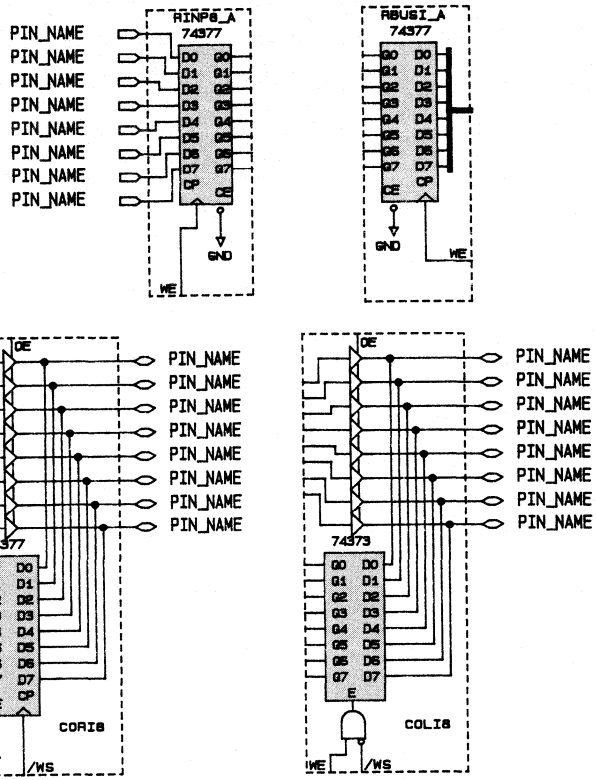


SSI FUNCTIONS

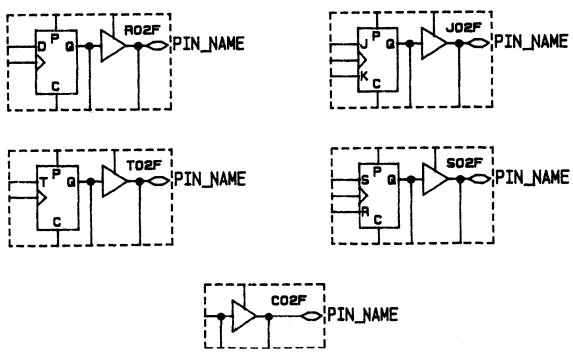


Note: Many of these SSI functions are identical to the primitive library elements. The SSI TTL part number equivalents are included for completeness.

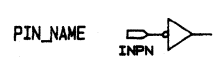
BUS PORTS



DUAL FEEDBACK



ACTIVE LOW INPUT



STATE MACHINE ENTRY FOR EPLDs

PLSME

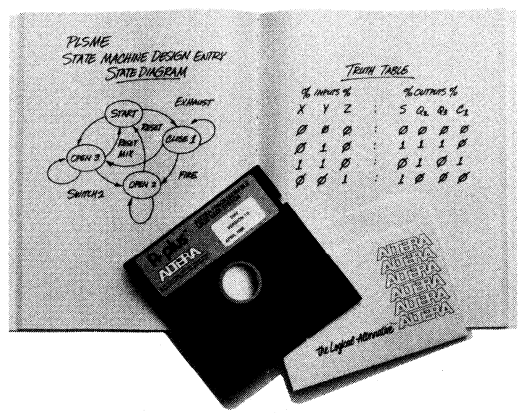
FEATURES

- Convenient form of design entry for state machine designs automatically transcribes high level descriptions into logical equivalents for automatic fitting and minimization into EPLDs.
- Standard format allows design to be merged with other state machines, schematic entry, Boolean equations, or netlist entry within a single EPLD.
- Sophisticated minimization algorithms in A+PLUS perform automatic reduction to improve device utilization. Automatic flip-flop selection optimizes state machine parameters.
- Human readable format eases the maintenance of complex designs, and documentation. Simple syntax is easy to learn.
- Multiple state machine definition allowed in one file. Flexible clock selection allows specification of any synchronous or asynchronous clock for any state machine.
- Outputs of state machines can be either conditionally or unconditionally defined.
- Truth table option allows the specification of random logic from functional definition.

FUNCTIONAL DESCRIPTION

State machines produce rugged designs with a minimum of logic. Unfortunately the development of state machines by hand involves a large amount of tedious work. With the advent of programmable logic, it became possible to implement very complicated state machines on a single chip since the logic array could implement very demanding logic structures, and the on-chip registers could serve as state registers. To make use of programmable logic, the designer was required to write out all the state equations and reduce them by hand. Because conventional programmable logic only offered inverted outputs, the designer had to apply De Morgan's inversion to the resultant logic by hand; a tedious time consuming operation. In the event that the design was incorrect or modified, the entire process had to be repeated.

Altera's PLSME and A+PLUS development system automatically transform high level state machine descriptions into device programming files. PLSME provides a state machine entry option in addition to the traditional entry methods currently available to A+PLUS (see fig. 1). Design information is entered using any standard (non document mode) text editor. It is then processed by the state machine converter to a standard Altera design file format (ADF). This common intermediate format allows the linking of multiple state machines, schematic, Boolean, or netlist entered design files, providing a rich development environment.



PLSME provides an easy to learn, and simple to use method of state machine design entry that frees the design engineer from the tedious hand conversion of high-level design information to logical requirements. PLSME automatically maps the design requirements into register and logic requirements which serve as input to the A+PLUS development software's automatic minimization and fitting algorithms.

REV.1.0

FEATURES OF SYNTAX

STATE MACHINE DEFINITION

The syntax of state machine description is both simple and powerful. A state machine is defined by clock selection, state assignments coupled to state variables and transition definition.

The state clock can be selected from any available clock on the device. This includes the dedicated synchronous clocks, and any asynchronous clock. Asynchronous clocks are signals created from logical signals within the EPLD. This option, available on most EPLD's, allows the definition of rich clocking structures on a single chip. Multiple state machines can be defined on one part, each with a different clock if so desired.

State assignments are defined in a tabular format by output variable only. These are coupled to state registers by position in the table. The choice of register type is not required. Altera's design processor will automatically select the best register type to support the implementation's selections.

Definition of state transitions is accomplished with a simple IF/ THEN/ ELSE construct. Transitions are defined to be mutually exclusive so that there are no ambiguities about next state values. The power on state is reset to an all low value, allowing the designer to provide reliable operation at system start-up. Outputs can be associated with states in the state machine definition or external to it. If defined internal to the state machine they can be unconditional, asserted on entry into a given state, or conditional, dependent on present state and external input signals or expressions. Outputs may be registered or combinatorial. The names associated with states can be used in logic equations outside the state machine definition, allowing easy interface to logic schematics.

Maintenance and modification of state machines is simple. High level modification of the IF/ THEN /ELSE statements allows redefinition of state transitions. Inclusion or deletion of states can be performed with similar simplicity. Additon or deletion of additional state variables, outputs, or inputs is supported. The high level descriptions are human readable. The understanding of complex logical structures becomes conceptually simple to support personnel, thus easing the maintenance of a complex design.

TRUTH TABLE DEFINITION

The syntax of truth table definition allows the high level description of logic requirements without Boolean equations. A truth table consists of input and output definition, and input and output pair specification. Valid input or output values or 0, 1 and X (don't care). Truth table outputs can be used as any Boolean statement can; as inputs to output primitives or logic. Such outputs can also be globally accessed outside the scope of their own file. See figure 3 for an example of truth table definition.

FIG. 1 STATE MACHINE DESIGN ENTRY

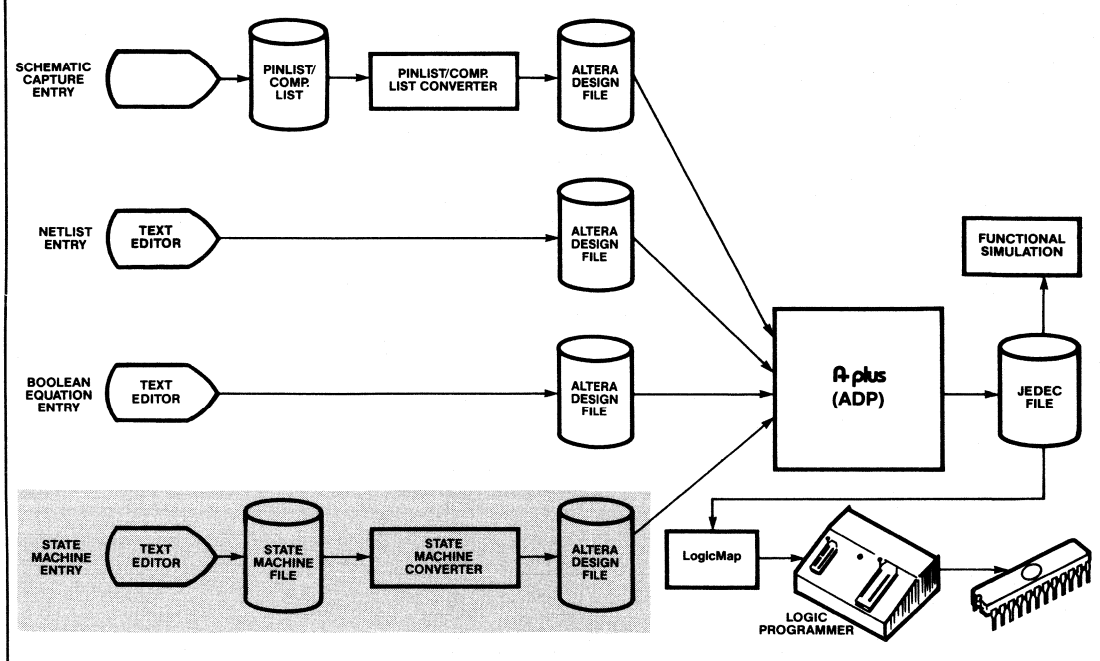
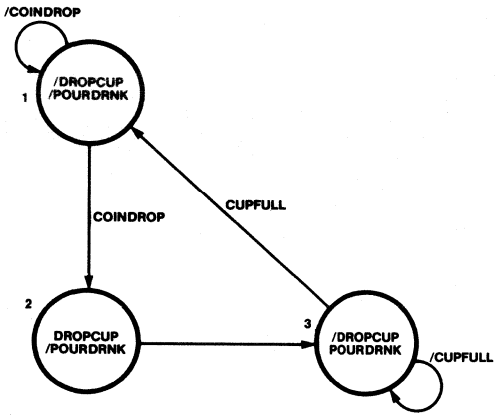


FIG. 2 STATE MACHINE EXAMPLE




```
MACHINE: dispenser
  CLOCK: CLK
  STATES: [DROPCUP  POURDRNK]
  S1      [   0         0    ]
  S2      [   1         0    ]
  S3      [   0         1    ]

S1:
  IF COINDROP THEN S2
  % No outputs %
S2:
  S3
S3:
  IF CUPFULL THEN S1
```

BOOLEAN EQUATION DEFINITION

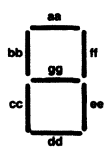
The Boolean equations section allows the standard definition of intermediate values which can be accessed by the state machine. This allows a high level description of otherwise discrete events, and eases the readability of the state machine definition.

INPUT/OUTPUT DEFINITION

The network section affords the designer control over the type of input and output structures that are desired within the device.

The combination of all the above entry options within PLSME provides a powerful working environment for the logic designer.

FIG. 3 TRUTH TABLE EXAMPLE



T-TAB:	q4	q3	q2	q1	:	aa	bb	cc	dd	ee	ff	gg	;
%0%	0	0	0	0	:	0	0	0	0	0	0	1	;
%1%	0	0	0	1	:	1	0	0	1	1	1	1	;
%2%	0	0	1	1	:	0	1	0	0	1	0	0	;
%3%	0	0	1	0	:	0	1	1	0	0	0	0	;
%4%	0	1	1	0	:	1	0	1	1	0	0	0	;
%5%	0	1	1	1	:	0	0	1	0	0	1	0	;
%6%	0	1	0	1	:	0	0	0	0	0	1	0	;
%7%	0	1	0	0	:	0	1	1	1	0	0	1	;
%8%	1	1	0	0	:	0	0	0	0	0	0	0	;
%9%	1	1	0	1	:	0	0	1	1	0	0	0	;
%A%	1	1	1	1	:	0	0	0	1	0	0	0	;
%B%	1	1	1	0	:	1	0	0	0	0	1	0	;
%C%	1	0	1	0	:	0	0	0	0	1	1	1	;
%D%	1	0	1	1	:	1	1	0	0	0	0	0	;
%E%	1	0	0	1	:	0	0	0	0	1	1	0	;
%F%	1	0	0	0	:	0	0	0	1	1	1	0	;

Truth tables offer an alternative to Boolean logic equations. In this example all of the logic requirements for a seven-segment display are expressed in a truth table instead of as a series of 7 equations. Reduction of terms is performed automatically to provide efficient functional equivalents.

SPECIFICATIONS

PLSME consists of:

SOFTWARE
— State Machine Converter (SMV) diskette and plastic slip cover.

DOCUMENTATION
— A+PLUS State Machine Entry supplement.

REQUIRED HARDWARE

PLSME requires an IBM Personal Computer, PC-XT, PC-AT, or compatible of running MS-DOS or PC-DOS version 2.0 or later. The configuration must have a 360KB doubled-sided, double-density disk drive and a hard disk drive. The system must have a minimum of 640KB.

FUNCTIONAL SIMULATOR PLFSIM

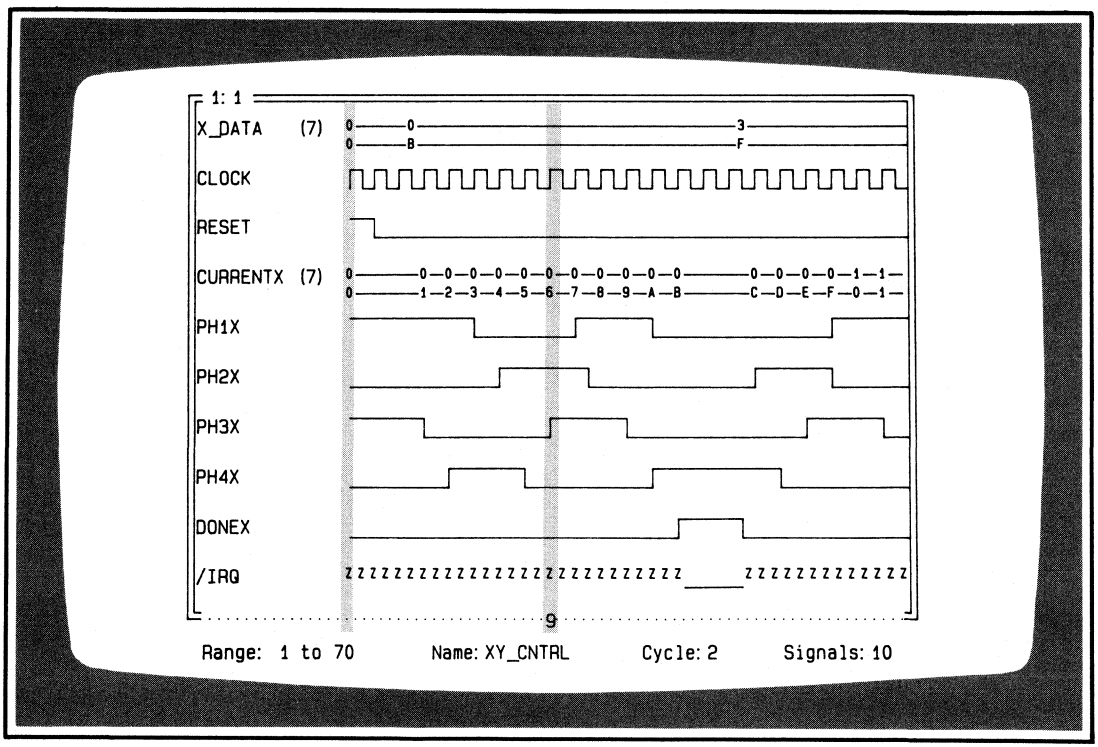
FEATURES

- Functional Simulation for Altera's entire family of EPLDs.
- Back-end integration with A+PLUS environment using JEDEC file for simulation.
- Easy definition of inputs using state tables, vector patterns or predefined patterns.
- Output formats include state table or graphic waveforms for on-screen display or hardcopy printout.
- Debugging ability with Break, Force, Save and Restore commands.
- Ability to access buried nodes within the design.
- Automatically computes the percent simulation coverage.

GENERAL DESCRIPTION

PLFSIM, the Altera Functional Simulator, provides a convenient and easy-to-use tool for testing the logical operation of any EPLD design. This software package requires the use of any general purpose text editor and is completely compatible with the A+PLUS development system. As a result, users may now enter designs, have them automatically fitted and optimized, then perform logic simulation without needing to commit a device to hardware.

In order to use PLFSIM, the user must have 3 files: a JEDEC file, a VECTOR file, and a COMMAND file. The JEDEC file is the design file created by the A+PLUS processor and contains all the logical information about the design. The VECTOR file contains the logic values that are to be applied to the inputs and is created with a text editor. A COMMAND file is used to tell PLFSIM what to do and when to do it. This "instruction list" may be created with a text



PLFSIM's interactive display of simulation results allows "logic-analyzer" like interaction with the Simulator.

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editor for a "batch run" or the user may choose to enter commands interactively from the keyboard.

The output of PLFSIM consists of graphical waveforms as well as formatted state tables which may be displayed or printed. In addition, a command log may be generated which will store an "instruction list" for future use.

EASY DEFINITION OF INPUT SIGNALS

PLFSIM is designed to allow flexible entry of input vectors. All input waveforms are defined in the VECTOR file. Standard state table entry is allowed as well as pattern entry for easy use of repetitious input waveforms. Legal input vectors include '1', '0', 'X' and 'Z' which allow complete simulation of the bidirectional architecture of the EPLD.

A set of inputs may be defined as a signal group which allows that group's input vector to be listed in hexadecimal, decimal, octal, or binary form. In addition, an input group can be given one of four predefined waveforms including Binary Count, Grey Code, Rotating Bit and Glitch Detector.

During simulation, the user can change between multiple VECTOR files to examine different aspects of the design as desired. Finally, simulation states from a given session can be "saved" and "restored" as initial conditions in a future session.

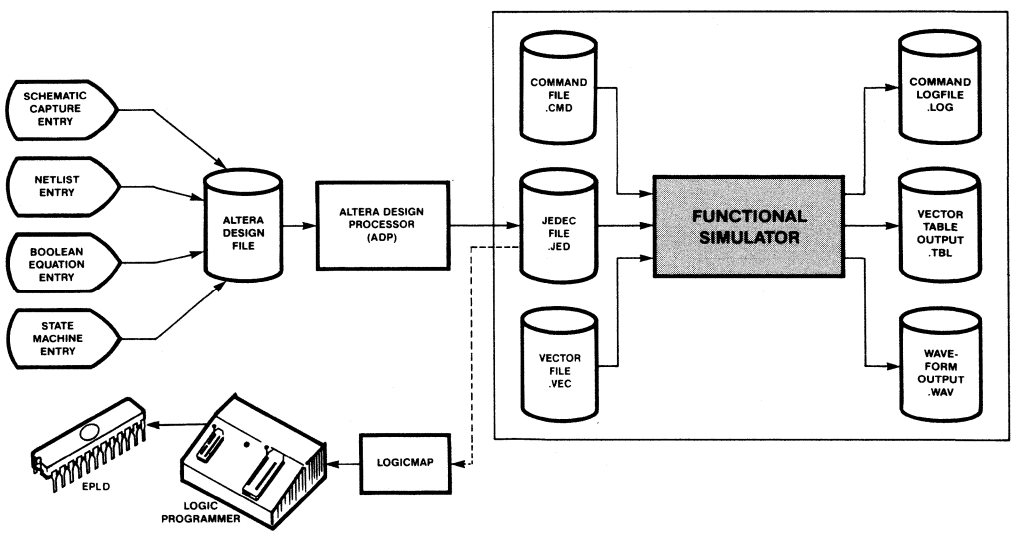
FLEXIBLE OUTPUT FORMATS

PLFSIM supports both waveform as well as tabular type outputs. The outputs formats are user-configured to show the logic states of input and output signals as well as buried nodes. The "simulation coverage" is calculated and included in the output file to indicate how thoroughly the design was exercised. Both output files can be shown on the screen or stored to a disk and printed for permanent documentation.

```
FSIM Version 1.1  11/20/86
JEDEC file : 74191.JED
EPLD part  : EP600


      C
      Y          D        R M
      C L        N        C N
      L D I C U G      Q O M
      E N N K P N      Q N X

        1 7 0 1 0 0 0 0 1
      1 1 7 1 0 0 F 0 1
        0 7 0 0 0 F 0 1
      2 0 7 1 0 0 7 1 0
        1 7 0 0 0 7 1 0
      3 1 9 1 0 0 8 1 0
        1 9 0 0 0 8 1 0
      4 1 9 1 0 0 9 1 0
        1 9 0 0 0 9 1 0
      5 1 9 1 0 0 A 1 0
        1 9 0 0 0 A 1 0
      6 1 9 1 0 0 B 1 0

Simulation cover : 72%
```

Tabular output for 74191 counter.

FUNCTIONAL SIMULATOR BLOCK DIAGRAM



POWERFUL COMMANDS

A complete set of simulation commands allows the user to check critical logic within a design in a succinct and straightforward manner. Users can specify commands to occur at particular events, such as during a given circuit condition or at an absolute simulation timestep. Users may force nodes to a chosen logic state to verify proper circuit behavior from any initial condition. The input waveforms from the VECTOR file can be superseded by another pattern at any point in time.

For debugging purposes simulation breakpoints can be set to halt execution when a specified event occurs. This "break" command provides designers the ability to detect illegal states. Once a break condition is met, a command sub-list is activated to provide status information or to enter into a separate procedure. So, for example, a break point might signal an illegal state, display the current output waveform on the screen, enter a legal state and continue with the simulation.

The commands may be entered interactively from the keyboard or may come from a pre-created command file. A command list that is entered interactively can be "logged" into a text file for future use. A command file can be called up at any point in the simulation process, including from another command file. This allows the nesting of command files so that, for example, a "break" command can execute a unique command file when a condition has been met.

CONTENTS

- Floppy disk containing all necessary software modules
- Inserts to A+PLUS User Manual for PLFSIM

SYSTEM REQUIREMENTS

- IBM XT, AT or compatible computers
- MS-DOS version 2.0 or later
- 640 Kbytes RAM
- Monochrome or Color monitor and card

SOFTWARE MAINTENANCE AGREEMENTS

- PLAESW-PC—12 month renewable maintenance contract for all PC-based Altera software. This contract covers the PLFSIM software.

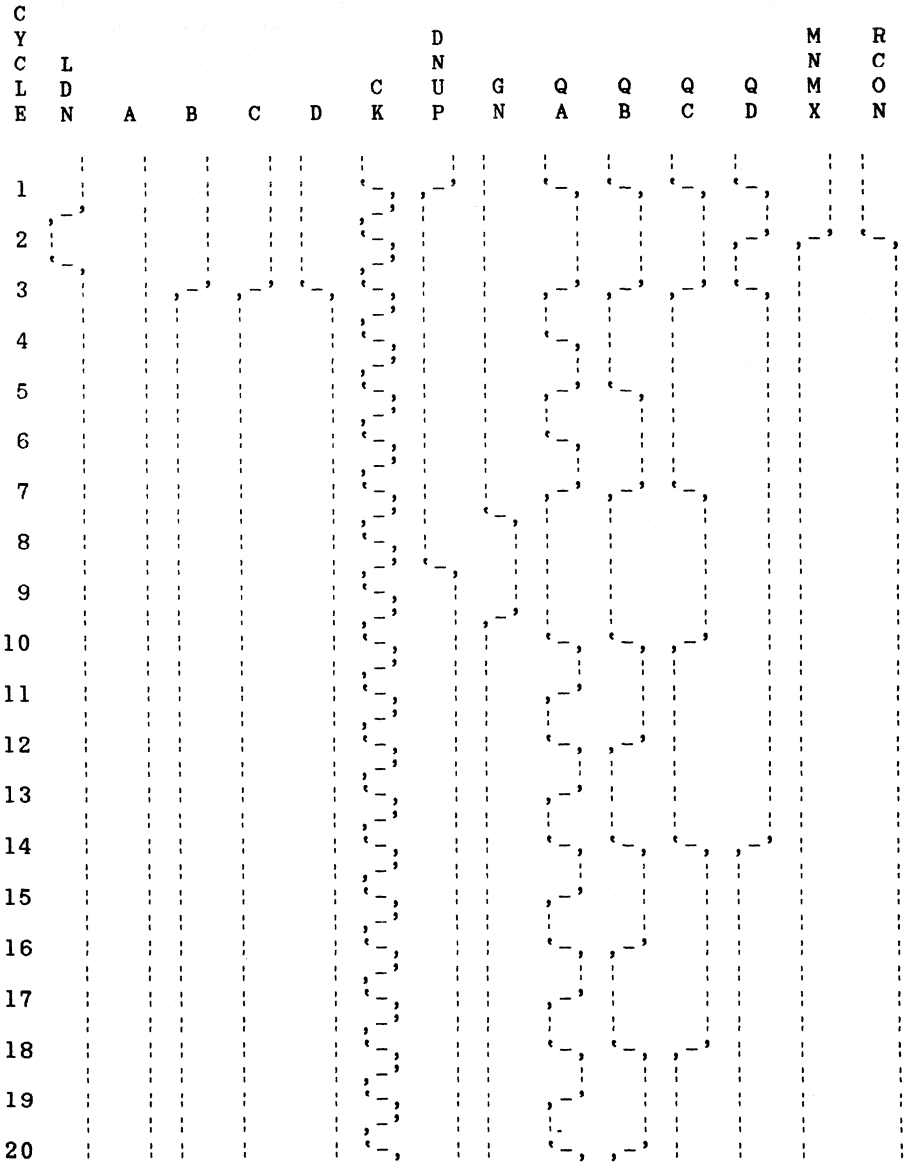
ORDERING INFORMATION

Order by product name: PLFSIM.

TABLE 1.
SIMULATION COMMANDS LISTED BY FUNCTION

FUNCTION	COMMAND
Node commands Set signals to specified logic levels.	FORCE INITIALIZE (INIT)
Information commands Provide data about commands, nodes and groups.	DESCRIBE (DESC) GROUP HELP STATUS SYMBOLS (SYMB)
Simulation control commands Control execution of the simulation.	BREAK CLEAR CONTINUE (CONT) QUIT SIMULATE (SIM)
Input commands Specify input to the simulator.	EXECUTE (EXEC) RESTORE (REST) SAVE VECTOR (VEC)
Output commands Specify the output format and display.	CYCLE DISPLAY (DISP) LOGFILE (LOG) PATTERN PLOT WATCH

```
FSIM Version 1.1 11/20/86
JEDEC file : 74191.JED
EPLD part  : EP600
```




```
Simulation cover : 87%
```

Waveform output example for 4-bit synchronous counter.

DEVELOPMENT SOFTWARE FOR SAM EPLDS

PLS-SAM

FEATURES

- Development software supporting Altera's Stand Alone Microsequencer (SAM) series of EPLDs
- State Machine Design Entry
- Assembly Language Design Entry
- User Definable Macros
- Interactive Functional Simulator with Virtual Logic Analyzer user interface
- Disassembler for examination of Assembly Code during simulation
- Fully supports Horizontal Cascading of multiple SAMs
- Runs on PC-XT, PC-AT, or compatible computers
- Complete support of device programming through Altera programming hardware
- Also available as a software only extension to existing Altera Development systems

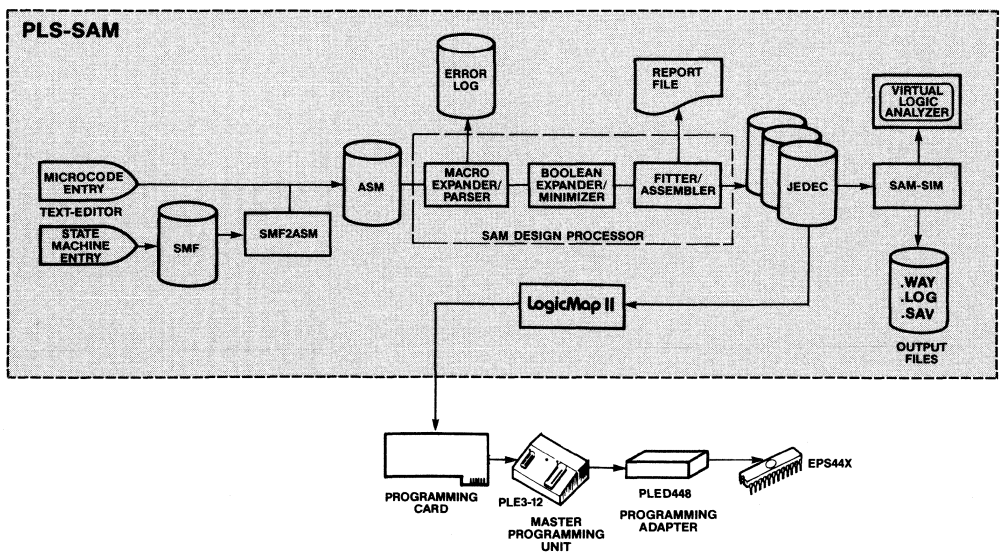
GENERAL DESCRIPTION

The Altera PLDS-SAM (Programmble Logic Development Software) represents a complete software solution to implementing State Machine and Microcoded applications into Altera's SAM family of Function-Specific EPLD's. PLS-SAM is a comprehensive, easy to use system that encompasses design entry with SAM+PLUS, design debugging with SAMSIM, and device programming with the Altera programming hardware.

The SAM+PLUS processing software accepts two forms of design entry and automatically generates an industry standard JEDEC file object code. SAMSIM is an interactive functional simulator created specifically for verification of State Machine and Microcoded designs implemented in SAM EPLDs.

For existing Altera PLDS or PLCAD users, PLS-SAM (Programmable Logic Software) is available as a software enhancement to their current system.

Figure 1. PLDS-SAM Block Diagram



FUNCTIONAL DESCRIPTION

Figure 1 shows a Block Diagram of the SAM+PLUS development system. Design entry with SAM+PLUS is done with either the Altera State Machine Input Language (ASMILE) or the Altera Assembly Language (ASM). With either method, a text-editor is used to create the input file. If the ASMILE language is used, a State Machine to Assembly converter will produce an Assembly Language file (ASM). The ASM file is passed on to the various modules that make up the SAM Design Processor (SDP). The SDP produces 3 outputs: an industry standard JEDEC file used to program the SAM EPLD, an Error Log file, and a Utilization Report file showing how the resources within the device have been used.

Once the JEDEC file is produced, the user may simulate the design using the SAMSIM functional simulator. SAMSIM provides an interactive design debugging environment. SAMSIM's Virtual Logic Analyzer provides on-screen examination of input and output waveforms and the Disassembler converts object code back into the original Assembly Language source code during simulation.

Horizontal cascading (using multiple SAM devices to increase the number of outputs) is fully supported including design entry, processing, simulation, and programming. The multiple SAM parts are listed in a single source file, and separate Report and JEDEC files are created for each.

Finally, the user can program the SAM device with the LogicMap software and programming hardware. Users who have access to an Altera development system may use the same hardware together with PLS-SAM software to program SAM devices through new adapters. For new users, PLDS-SAM, includes all the programming hardware and software required to program the EPS44x parts using a PC-XT, PC-AT, or compatible system.

STATE MACHINE DESIGN ENTRY

The SAM+PLUS (SAM Programmable Logic User Software) software supports high-level state machine design entry through the Altera State Machine Input Language (ASMILE). A designer uses this language with any standard text-editor to create a text file that describes the desired state machine. The SMF2ASM convertor will convert the State Machine File into an equivalent Assembly Language File before passing it to the SAM Design Processor.

ASMILE provides a simple yet comprehensive means of converting a conceptual state diagram into a simple text description. Figure 2 shows the state diagram for a 68020 bus arbiter. Each bubble represents a state, the values within the bubbles represent the output values for that state, and the expressions on the arrows represent the conditional branches between states.

Figure 2. State Diagram for 68020 Bus Arbiter

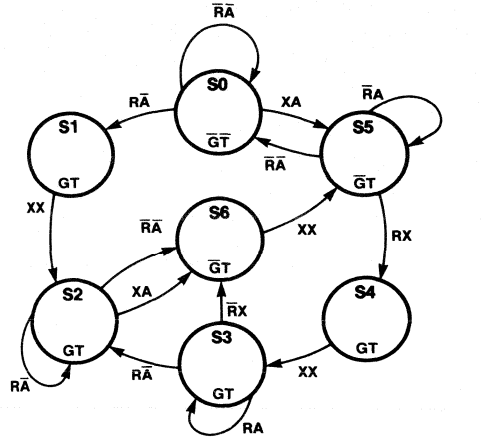


Figure 3. State Machine Input File

```
DESIGNER NAME
COMPANY NAME
4/1/87
68020 Bus Arbitration Controller for SAM


PART:EPS444

INPUTS: REQUEST ACK

OUTPUTS: GRANT TRISTATE

MACHINE: BUSARBITER

CLOCK: CLK

% The State table defines the outputs
  for each state                      %

STATES: [GRANT TRISTATE]

  S0     [  0       0     ]
  S1     [  1       1     ]
  S2     [  1       1     ]
  S3     [  1       1     ]
  S4     [  1       1     ]
  S5     [  0       1     ]
  S6     [  0       1     ]

% Transition Specifications follow %

S0: IF REQUEST*/ACK THEN S1
    IF ACK THEN S5
    S0

S1: S2

S2: IF /REQUEST*/ACK + ACK THEN S6
    S2    % Implied ELSE  %

S3: IF /REQUEST THEN S6
    IF REQUEST*/ACK THEN S2
    S3

S4: S3

S5: IF /REQUEST*/ACK THEN S0
    IF REQUEST THEN S4
    S5

S6: S5

END$
```

Figure 3 shows the Altera State Machine Input Language representation of the same state machine. Notice that the states and their respective outputs have been defined in the STATES section using a truth table format. The transitions between the states have been defined with a simple IF-THEN construct. Once this file is created, it can be passed on to the SMF2ASM converter with no further modifications.

ASSEMBLY LANGUAGE DESIGN ENTRY

Direct Assembly Language design entry is also available for those who prefer to approach SAM as a microcoded controller. This entry method provides access to the advanced features of the SAM family including the on-chip Stack and Loop Counter. There are 13 instructions that directly control such functions as multi-way branching, sub-routines, nested for-next loops, and dispatch calls (jumping to an externally specified address).

In addition, user-defined Macros are available which allow users to define their own instruction mnemonics. This provides a higher level design entry approach. Macros are also useful for defining output values for various output fields so that the designer does not have to work at the binary level.

Figure 4 shows an example of an Assembly Language file. In this file, Macros have been used to define the 7 new instructions "GOTOS0" through "GOTOS6".

DESIGN PROCESSOR

The SAM Design Processor (SDP) takes an Assembly Language file and creates an optimized JEDEC file for the targeted device. The SDP first expands Macros that have been defined by the user. It then parses the design, listing any syntax or connection errors in an Error Log file. Next it minimizes the Boolean expressions that define the transition conditions. Finally, it fits the design into the SAM EPLDs, generating a separate JEDEC file for each. A Utilization Report file is also produced showing how and where the various instructions were implemented.

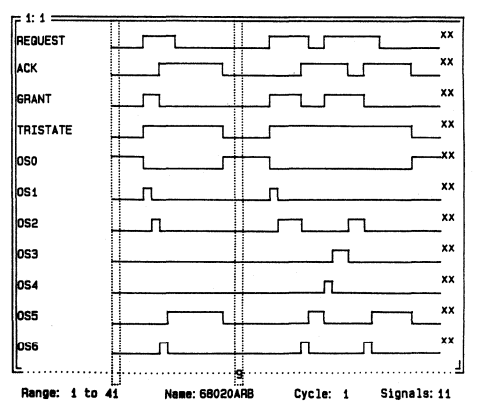
FUNCTIONAL SIMULATION—SAMSIM

Once a design has been processed and a JEDEC file created, it can be simulated with the SAMSIM Functional Simulator. SAMSIM provides a comprehensive design debugging environment. The Virtual Logic Analyzer displays the input and output waveforms interactively providing such features as multiple zoom levels, split screen, and differential time display. The internal state of the SAM device, including the Stack and Counter, can be examined and modified at will. In addition, an on-line disassembler converts the actual object code back into the original Assembly Language source code.

Figure 4. Assembly Language Input File

```
DESIGNER NAME
COMPANY NAME
4/1/87
68020 Bus Arbitration Controller for SAM

PART: EPS444

INPUTS: REQUEST ACK

OUTPUTS: GRANT TRISTATE

MACROS:
GOTOS0 = "[00] JUMP S0"
GOTOS1 = "[11] JUMP S1"
GOTOS2 = "[11] JUMP S2"
GOTOS3 = "[11] JUMP S3"
GOTOS4 = "[11] JUMP S4"
GOTOS5 = "[01] JUMP S5"
GOTOS6 = "[01] JUMP S6"

PROGRAM:

0D:   GOTOS0;

S0:   IF REQUEST*/ACK THEN GOTOS1;
      ELSEIF ACK THEN GOTOS5;
      ELSE GOTOS0;

S1:   GOTOS2;

S2:   IF /REQUEST*/ACK+ACK THEN GOTOS6;
      ELSE GOTOS2;

S3:   IF /REQUEST THEN GOTOS6;
      ELSEIF REQUEST*/ACK THEN GOTOS2;
      ELSE GOTOS3;

S4:   GOTOS3;

S5:   IF /REQUEST*/ACK THEN GOTOS0;
      ELSEIF REQUEST THEN GOTOS4;
      ELSE GOTOS5;

S6:   GOTOS5;

END$
```

Figure 5. Screen from Virtual Logic Analyzer



PROGRAMMING HARDWARE AND SOFTWARE

LogicMap II is the programming software used to program the entire EPLD family, including the SAM series. The program fully calibrates the programming environment and checks out the programming hardware when initiated. Programming hardware consists of a software-configured programming card that occupies a single slot in an IBM-PC or compatible computer (PLP4), a Master Programming Unit (PLE3-12), and a programming adapter (PLED448 or PLEJ448). LogicMap works with this hardware to program or verify a SAM EPLD.

PLS-SAM is provided for existing owners of Altera PLDS or PLCAD development systems that include a PLP4 programming card and a PLE3-12 Master Programming Unit. PLDS-SAM users receive all the required programming hardware and software. The PLP4 programming card and the PLE3-12 Master Programming Unit are compatible with the entire family of EPLDs.

PLS-SAM CONTENTS

- Floppy diskettes containing all the programs and files for SAM+PLUS software
  - — State Machine Entry
  - — Assembly Language Entry
  - — SAM Design Processor
  - — SAM-SIM Functional Simulator
  - — LogicMap II
- User Manual

PLS-SAM HARDWARE ENHANCEMENTS

- PLP4 Programming Card—Software controlled programming card which fits in a single expansion slot of an IBM-PC or compatible.
- PLE3-12 Master Programming Unit and cable
- PLED448—Programming adapter for the EPS444 and EPS448 DIP packages
- PLEJ448—Programming adapter for the EPS448 JLCC/PLCC packages

SYSTEM REQUIREMENTS

- IBM XT, AT or compatible machine
- Monochrome, CGA, EGA, or Hercules display
- 640K bytes of main memory
- 10M byte hard disk drive and floppy drive
- DOS versions 2.0 or later release

EXTENDED SOFTWARE WARRANTY

- PLAESW-PC—12 month renewable warranty for all PC-based Altera software. This contract covers all software contained within PLS-SAM or PLDS-SAM as well as all other Altera software owned by the registered user. PLAESW-PC includes automatic upgrade to each new revision of Altera software and guarantees software support for new SAM EPLDs introduced by Altera. It also includes toll-free hotline and 24 hour modem interface to Altera Electronic Bulletin Service.

ORDERING INFORMATION

- Order by product number: PLDS-SAM
  PLS-SAM

3

PCAD PC-CAPS INTERFACE SOFTWARE TO ALTERA A+PLUS DEVELOPMENT SYSTEM SOFTWARE

PLE2

PLE2 CONTENTS

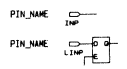
- Altera schematic symbol library for PC-CAPS.
- Altera interface between A+PLUS and PC-CAPS.
- Insert to A+PLUS Reference Manual.

ORDER INFORMATION

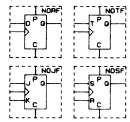
PLE2

PRIMITIVE SYMBOL LIBRARY

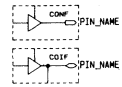
INPUT BUFFERS



FLIPFLOPS



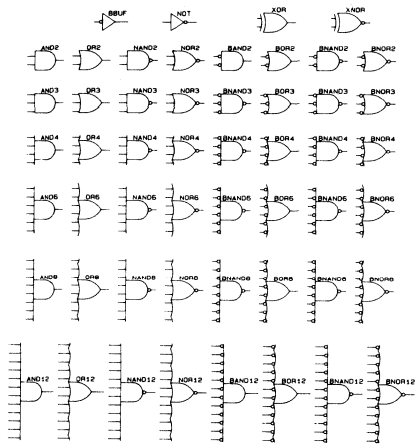
OUTPUT BUFFERS



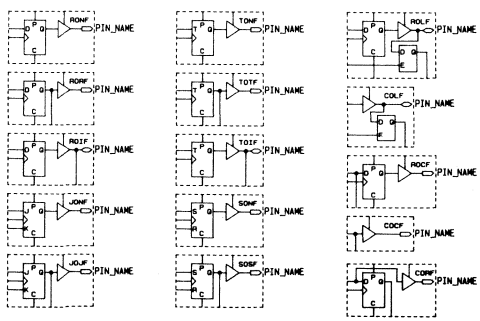
CLOCK BUFFER

INTERNAL BUFFER

BASIC GATES



COMPOUND PRIMITIVES



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FUTURENET DASH INTERFACE SOFTWARE TO ALTERA A+PLUS DEVELOPMENT SYSTEM SOFTWARE

PLE20

PLE20 CONTENTS

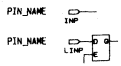
- Altera schematic symbol library for DASH-2, -3, -4C, -4M.
- Interface between A+PLUS and DASH-2, -3, -4C, -4M.
- Insert to A+PLUS Reference Manual.

ORDER INFORMATION

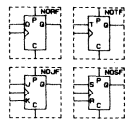
PLE20

PRIMITIVE SYMBOL LIBRARY

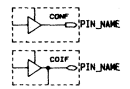
INPUT BUFFERS



FLIPFLOPS



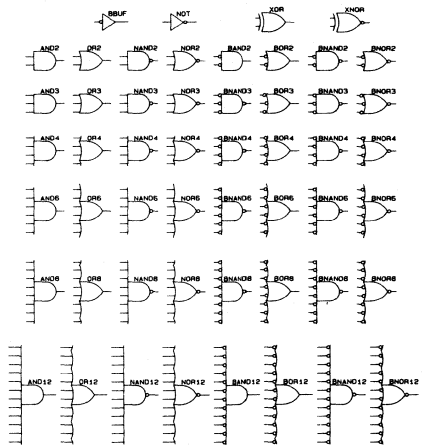
OUTPUT BUFFERS



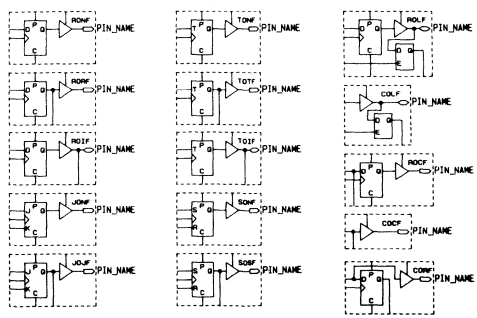
CLOCK BUFFER

INTERNAL BUFFER

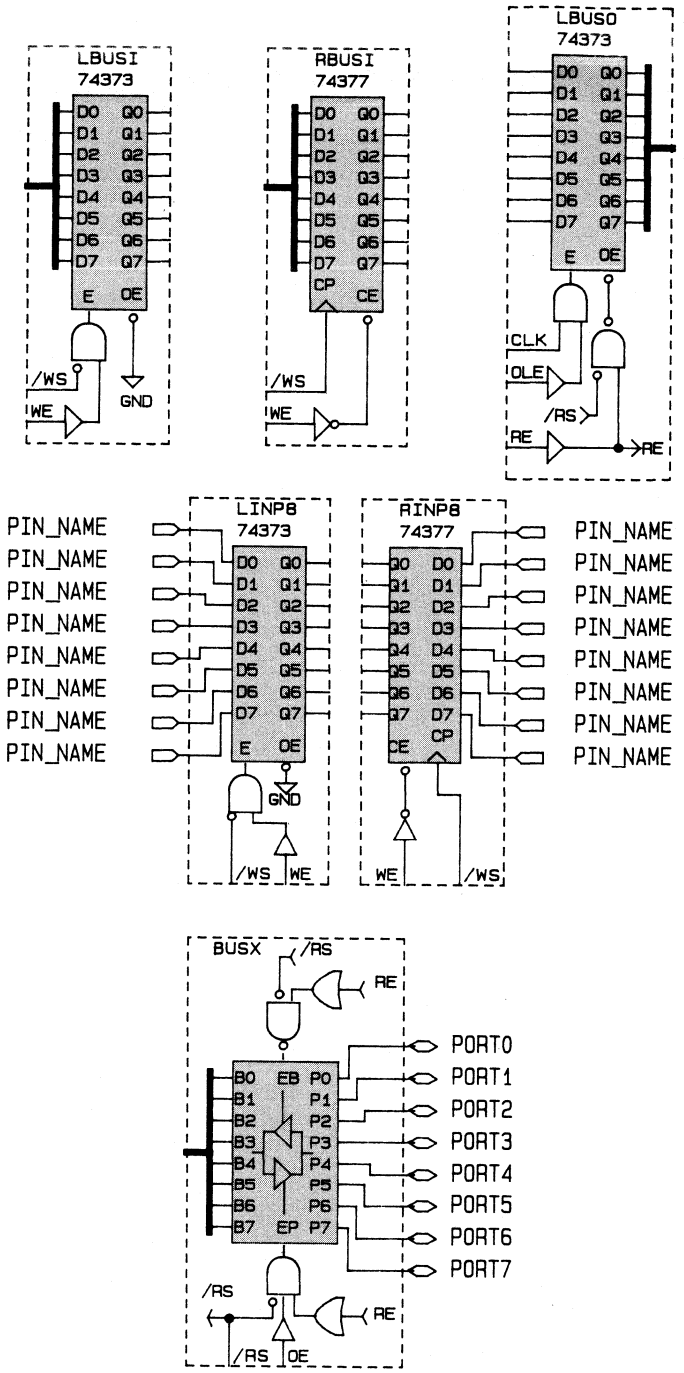
BASIC GATES



COMPOUND PRIMITIVES



BUSTER PRIMITIVES



PLAESW-PC
EXTENDED SOFTWARE WARRANTY

FEATURES

- Automatic update for new EPLDs
- Applications support Hotline
- Modem access to design library
- Discounts on software options
- Design assistance with modem design transfer support

GENERAL DESCRIPTION

These software maintenance and support products provide the development system user access to the latest revisions of software. Development software is subject to periodic upgrade to provide new features and to support new EPLDs. These products provide a simple approach to ensure that your development system is fully up to date and ensures you are able to use the latest EPLD technology. The support includes to applications assistance for design work with Hotline access to applications engineers. Designs can be transferred to Altera via a 24-hour auto-answer dial-up modem service.

An extensive design library can also be accessed via this modem link.

TTL AND APPLICATION DESIGN LIBRARY

The Altera TTL library which contains over 100 logic designs. These are intended as practical examples of small circuits implemented in EPLDs. The designs in the library contain many techniques that may be useful when developing more complex circuits.

The complete library contains schematic drawings, and their Boolean algebra equivalents in the Altera Design File format (ADF). Subscribers to the A+PLUS upgrade and maintenance package have free access to this design database.

OPTIONS:

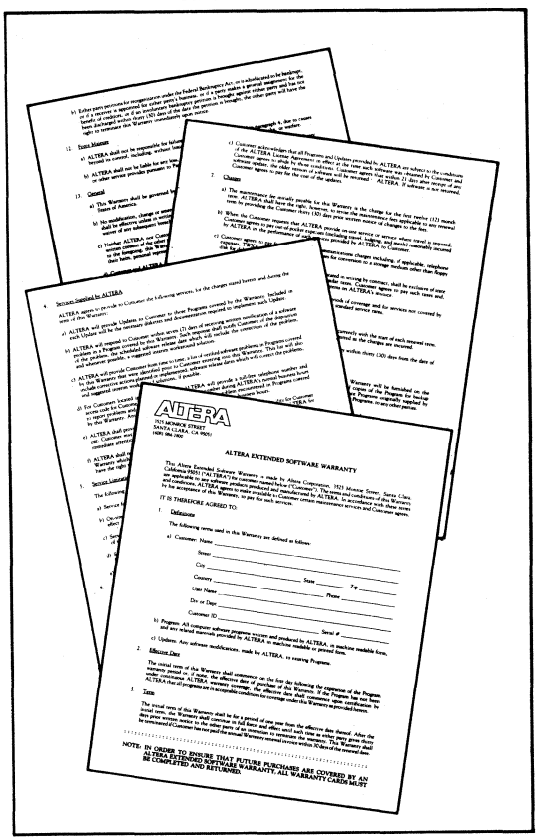
PLAESW-PC Extended Software PLAESW Warranty for all Altera PC based software applications

Access: 1200 Baud Dial-Up Auto-Answer modem. Password access only.

Duration: 12 months, renewable.

Recommended computer configuration:

- IBM XT or AT and compatible machines
- 1200 Baud modem (212A)
- Color graphics or Enhanced graphics display
- 640k bytes of main memory
- 10M byte hard disk drive and floppy-disk drive
- MS-DOS or PC-DOS version 3.2 or later releases
- Full-card slot for programming card



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PLE3-12 PROGRAMMING UNIT PLE3-12

FEATURES

- Master programming unit for all Altera EPLDs.
- Directly supports Altera EP310, EP320, EP1200, and EP1210 DIP EPLDs.
- Optionally supports all other EPLDs via plug-in adaptors.
- Fully compatible with Altera Programming Card.
- Zero-Insertion-Force sockets for easy device insertion and extraction.
- Indicator LED shows when unit is active.

PLE3-12 PROGRAMMING SUPPORT

EPLD	PACKAGE	ADAPTOR
EP310	DIP	DIRECT
EP320	DIP	DIRECT
EP600/EP610	DIP	PLED600
	J-LEAD	PLEJ600
EP900/EP910	DIP	PLED900
	J-LEAD	PLEJ900
EP1200	DIP	DIRECT
EP1210	DIP	DIRECT
	J-LEAD	PLEJ1210
EP1800/EP1810	J-LEAD	PLEJ1800
	PGA	PLEG1800
EPS448	DIP	PLED448
	J-LEAD	PLEJ448
EPS444	DIP	PLED448
EPB1400	DIP	PLED1400
	J-LEAD	PLEJ1400

GENERAL DESCRIPTION

The Altera PLE3-12 Master Programming Unit is a hardware module capable of programming all Altera EPLDs. The PLE3-12 is designed to interface only with the Altera PC-based programming card. This programming card (included in a PLDS2 or PLCAD system) generates all programming waveforms and voltages. Thus, the PLE3-12 requires no additional power supply.

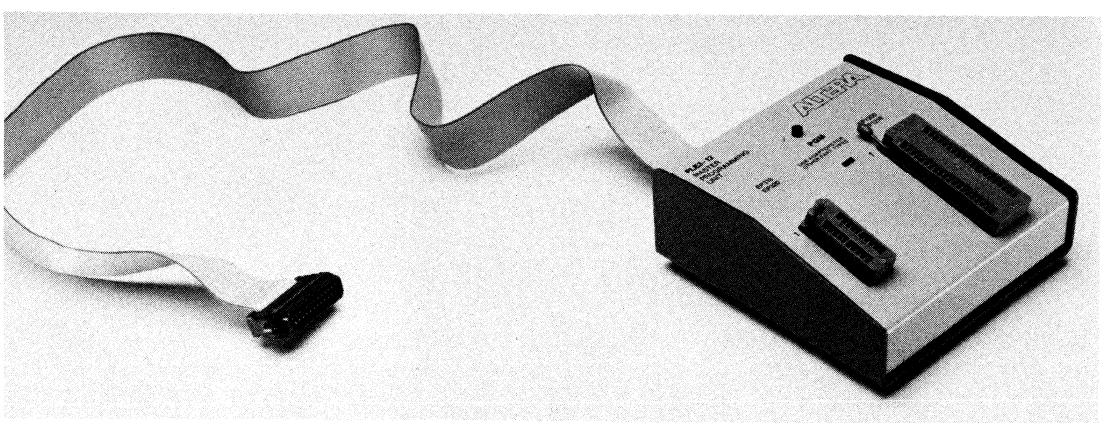
The PLE3-12 contains both a 20 pin (300 mil) and 40 pin (600 mil) zero-insertion-force sockets. The unit inclues a 30 inch ribbon cable terminated with a 25 pin D-type connector. Programming information is transmitted from the Altera Programming card (located in any full expansion slot of the PC) through the ribbon cable to the PLE3-12 programming unit. A programming indicator lamp is illuminated when the unit is active.

The PLE3-12 directly supports the EP310, EP320, EP1200, and EP1210 EPLDs (DIP packages only). The module also serves as the base unit for programming all other Altera EPLDs. Programming adaptors supporting each EPLD (DIP, J-Lead, and PGA packages) plug directly into the PLE3-12 module.

The PLE3-12 is included in the Altera PLDS2, PLCAD4, PLDS-SAM, and PLCAD-SUPREME development systems.

ORDERING INFORMATION

Order by product number: PLE3-12



REV. 2.0

PLED/J/G PROGRAMMING ADAPTORS PLED/J/G

FEATURES

- Programming adaptors for Altera EPS444, EPS448, EP600/EP610, EP900/EP910, EP1210, EPB1400 and EP1800/EP1810 EPLDs.
- Plugs directly into PLE3-12 Master Programming Unit.
- Zero-Insertion-Force sockets for easy device insertion and extraction.

ADAPTOR SUPPORT

EPLD	PACKAGE	ADAPTOR	BASE-UNIT
EPS444	DIP	PLED448	PLE3-12
EPS448	DIP	PLED448	PLE3-12
	J-LEAD	PLEJ448	PLE3-12
EP600/	DIP	PLED600	PLE3-12
EP610	J-LEAD	PLEJ600	PLE3-12
EP900/	DIP	PLED900	PLE3-12
EP910	J-LEAD	PLEJ900	PLE3-12
EP1210	J-LEAD	PLEJ1210	PLE3-12
EPB1400	DIP	PLED1400	PLE3-12
	J-LEAD	PLEJ1400	PLE3-12
EP1800/	J-LEAD	PLEJ1800	PLE3-12
EP1810	PGA	PLEG1800	PLE3-12

GENERAL DESCRIPTION

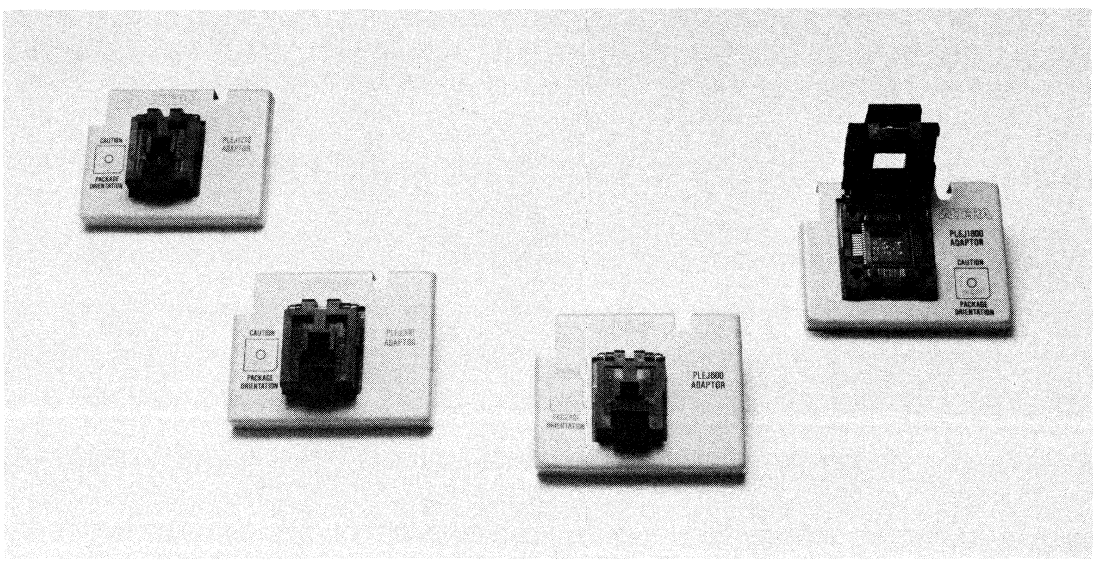
The Altera PLED/J/G 448, 600, 900, 1210, 1400 and 1800 are enhancement products allowing device programming to Altera EPLDs which are not directly supported by the PLE3-12 Master Programming Unit or the Multi-Host Programmer (VAX environment only).

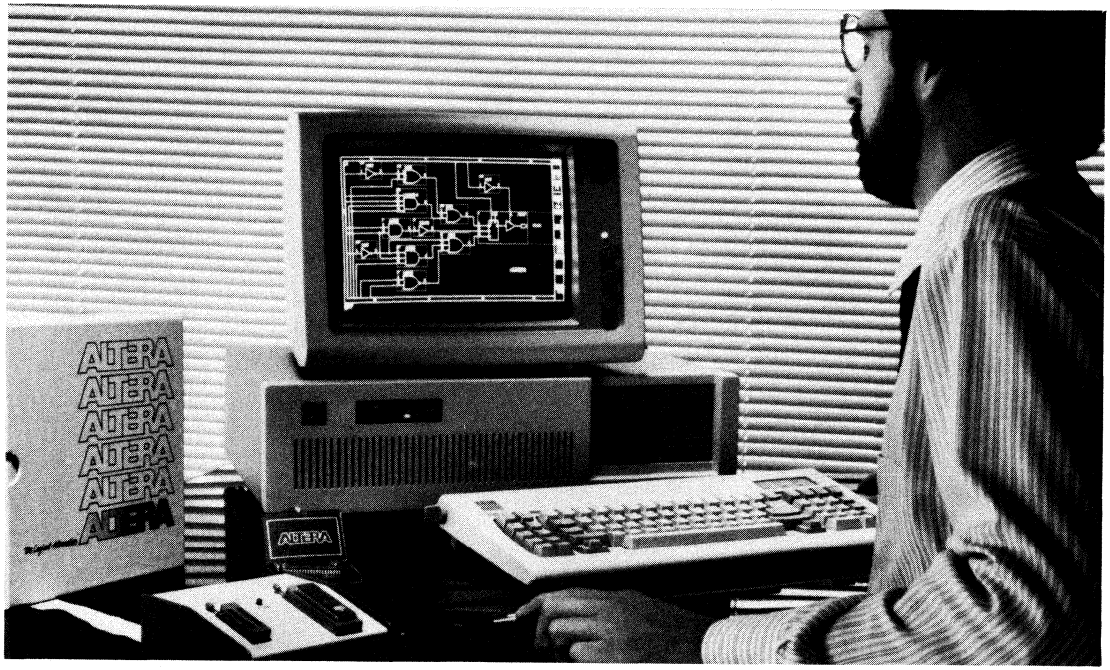
Each adaptor contains a zero-insertion-force DIP, J-lead, or PGA socket. The adaptors plug directly into the PLE3-12 or MHP. The PLE3-12 and MHP serve as base units by suppling programming waveforms and voltages to the adaptors.

ORDERING INFORMATION

Order by product number:

PLED448
PLEJ448
PLED600
PLEJ600
PLED900
PLEJ900
PLEJ1210
PLED1400
PLEJ1400
PLEJ1800
PLEG1800

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GENERAL INFORMATION

PAGE NO.

4

APPLICATION LITERATURE

This page contains a listing of all current application notes and application briefs. Application notes explore subjects more fully than an application brief. This listing covers current releases. Omitted numbers reference obsolete or unreleased publications. For an up-to-the-minute list and access to application design data call the Altera electronic bulletin board at:

(408) 249-1100

APPLICATION NOTE/BRIEF	TITLE
AN 1	Introduction to EPLDs
AN 2	Replacing 20 pin PALs
AN 3	Memory interfacing with EPLDs
AN 6	High Speed custom UART
AN 7	Introduction to State Machine Design
AN 8	EPLD technology and design recommendations
AN 9	Metastability characteristics of EPLDs
AN 10	SAM Application using State Machine Design Entry
AN 11	High-End SAM Applications Using Microassembler Design Entry
AN 12	Microprocessor Peripheral Design with BUSTER
AB 3	Manchester Encoder/Decoder
AB 4	T1 serial transmitter
AB 5	Single chip signature analyzer
AB 8	Efficient counter design with Toggle flip-flops
AB 9	Designing asynchronous latches with EPLDs
AB 10	Counter design using the EP1210
AB 11	16 Bit Up/Down counter with Left/Right shift register
AB 13	Design boundaries of the EP1210
AB 14	State Machine design entry
AB 15	Monostable, RC & XTAL oscillator designs in EPLDs
AB 17	State machine design guidelines
AB 18	Partitioning state machines
AB 19	Schmitt trigger inputs in EPLDs
AB 20	EP1800 X-Y position controller
AB 23	Multiplier circuits in EPLDs
AB 24	Functional simulation of EPLD designs using PLFSIM
AB 25	Successive approximation register design using the EP600
AB 26	Serial DATA FIFO Design in the EP1800
AB 27	EP1800 as a Bar Code Decoder
AB 28	How programmable flip-flops work in EPLDs
AB 34	Designing with MacroFunctions
AB 39	Implementing asynchronous Set using asynchronous Clear
AB 40	Power supply sequencing for EPLDs
AB 43	Converting PAL designs to EP320 EPLD
AB 44	The Altera MacroFunction library
AB 45	Testing Plastic OTP EPLDs
AB 46	Sockets and Prototyping hardware for EPLDs
AB 51	Total dose gamma radiation hardness of Altera EPLDs
AB 52	Low power EPLD guidelines
AB 54	EPLD timing simulation
AB 55	Using Dual Feedback in the EP1800
AB 56	Production Programming Specification

All EPLDs manufactured by Altera are supported by the A+PLUS development system and by third party programmer manufacturers.

Third Party programmer manufacturers that support Altera EPLDs may be contacted at the following addresses. They will be able to tell you the specific programmer model that supports Altera EPLDs.

Data I/O
10525 Willows Road N.E.
P.O. Box 97046
Redmond, Washington
98073-9746
United States
phone (206) 881-6444

World Trade Centre
Strawinskylaan 633
1077 XX Amsterdam
The Netherlands
phone (20) 622866

Stag Electronic Designs
Tewin Court
Welwyn Garden City
Hertfordshire AL7 1AU
United Kingdom
phone (07073) 32148

528-5 Weddell Drive
Sunnyvale, California 94089
United States
phone (408) 745-1991

Valley Data Sciences
Charleston Business Park
2426 Charleston Road
Mountain View, California 94043
phone (415) 968-2900

Varix
122 Spanish Village suite 608
Dallas, Texas 75248
phone (214) 437-0777

OAE
676 West Wilson Avenue
Glendale, California 91203
phone (818) 240-0080

Logical Devices
1321 North West 65th Place
Fort Lauderdale, Florida 33309
phone (305) 974-0975

Digelec Inc.
1602 Lawrence Avenue suite 113
Ocean, New Jersey 07712
phone (201) 493-2420

Elan Digital Systems Ltd.
16-20 Kelvin Way
Crawley, West Sussex
England
RH10 2TS

Japan Macnics Corp.
516 Imaiminami-Cho, Nakahara-Ku
Kawasaki-City, 211
Japan
phone 044-711-0022

Minato Electronics Inc.
4105 Minami Yamada-Cho
Kohoku-Ku, Yokohama 223
Japan

Digitronics Israel Ltd.
25 Galgaley Haplada Street
Herzliya B'
Israel
46722

Kontron Messtechnik GMBH
Breslauer Strasse 2,8057
Eching B. Munchen
West Germany
phone 89-3-19-01-374

AVAL Corporation
11 Deansgrange Ind. Estate
Deansgrange County Dublin
Ireland
850533

Sunrise Electronics
524 South Vermont Avenue
Glendora, California 91740
phone (818) 914-1926

Note: Altera assumes no responsibility for the suitability nor accuracy of third party programming equipment.

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Altera EPLDs should be programmed using data formatted within the JEDEC recommended standard for PLD object code. To obtain electrical programming information for programming Altera EPLDs from the JEDEC format write to:

Applications Department
(EPLD programming data)
Altera Corporation
3525 Monroe Street
Santa Clara, California 95051
United States

Copies of the appropriate JEDEC standard:

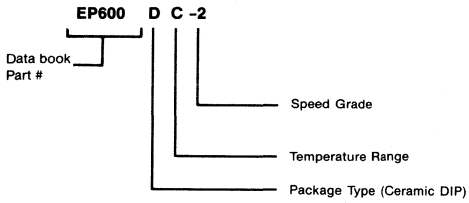
JEDEC Standard No.3 (JC-42.1)

may be obtained from the following address:

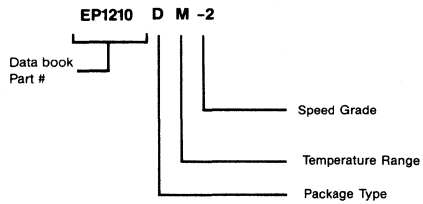
JEDEC Executive Secretary
Electronics Industries Association
2001 Eye Street N.W.
Washington, D.C. 20006
United States

Some examples of ordering various package and electrical as well as temperature grades are given below.

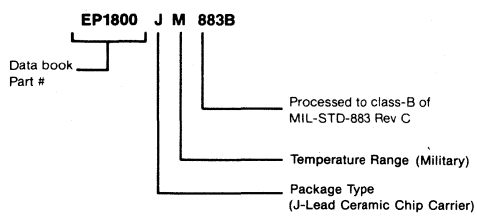
a) **Level-1 Product:**



b) **Level-2 Product:**



c) **Level-B, MIL-STD-883C:**



DEVELOPMENT SYSTEMS/SOFTWARE ORDERING INFORMATION

All development systems and software products should be ordered by their data sheet nomenclature. No other codes are assigned. Some examples are listed.

SYSTEM DESIGNATION	ORDER BY
PLDS 2	Same designation
PLCAD 4	Same designation
PLE 40	Same designation

PRODUCT CODE SUMMARY AND ORDERING INFORMATION.

PACKAGE CODES:

PACKAGE TYPE	MARKING/ORDERING LETTER DESIGNATOR
CERAMIC DIP	D
PLASTIC MOLDED DIP	P
CERAMIC J-LEAD CHIP CARRIER	J
PLASTIC MOLDED J-LEAD CHIP CARRIER	L
CERAMIC PIN GRID ARRAY	G

PRODUCT GRADES:

APPLICATION	TEMPERATURE RANGE	MARKING DESIG-NATOR
COMMERCIAL	0° C TO + 70° C	C
AUTOMOTIVE/ INDUSTRIAL	-40° C TO + 85° C	I
MILITARY	-55° C TO +125° C	M
MIL-STD-883C CLASS-B	-55° C TO +125° C	883 B

Notes:

For specific package/grade/speed combinations that are available, please refer to product listings or call Altera marketing department.

(408) 984-2805 x 101

QUALITY SYSTEMS DESCRIPTION

To produce good quality products, a well defined plan or a system of controls and monitors is the first step. This is particularly important for a growing organization. Recognition of this fact has led to the Altera system of quality controls that is represented in Figure 1 below.

It is obvious from Figure 1 that for a total quality control program, all aspects of a product flow need documentation, controls, training and audits. This is the fundamental aspect of Altera's quality program. Some of the major aspects of this program are described in the following sections.

DOCUMENT CONTROL

Altera's Document Control department has three basic functions.

DRAWING AND SPECIFICATION CONTROL

Up-to-date drawings and specifications related to materials, processes, testing, products and subcontractors are maintained by Document Control Department. A numbering system identifies each document by function, category and revision status.

CHANGE CONTROL

Once a product, process or material is released to production, any change in specification or drawings is governed by a change control procedure. All changes have to be justified with reasons and supporting data. The change is implemented only if approved by the appropriate functional groups including customers when applicable. A history of all changes is maintained by document control.

RECORDS MANAGEMENT

For MIL-STD-883 specification products, all records of inspections, screenings, qualification plans, quality conformance inspections and audits are retained for a period of five years.

TRAINING

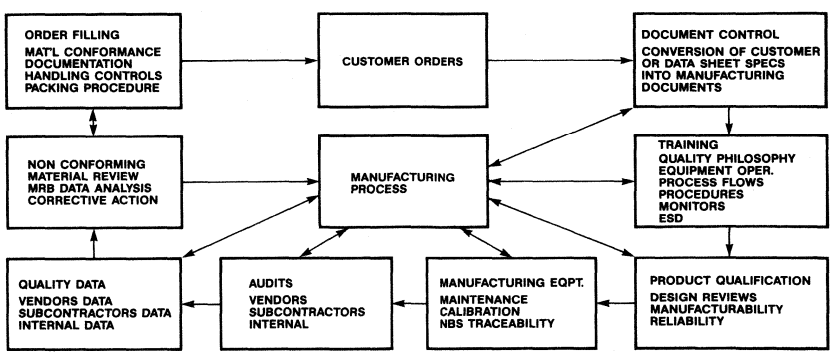
Training is an integral part of Altera operations and encompasses the following aspects.

- Selection of personnel based on specific work experience and education.
- Orientation to Altera's Product Assurance Program.
- On the job training for assigned operations. This includes operating procedures, inspection criteria and data recording.
- Qualification/disqualification at the end of a probationary period.
- Records of training.
- Periodic re-training & update of records.

PRODUCT QUALIFICATION

Every Altera product undergoes an extensive series of qualification and characterization tests. These include (but are not limited to) such tests as electrical characterization, life tests, ESD and package qualification. These tests are described in more detail in the product qualification section.

FIG. 1



MAINTENANCE AND CALIBRATION

Any electrical, thermal or physical measuring and test instrument that is used in manufacturing or evaluating Altera products is subject to periodic preventive maintenance and calibration. The calibration standards are traceable to the National Bureau of Standards.

Calibration status is indicated on each piece of equipment by a calibration sticker. Equipment not needing calibration or for reference only is so indicated by a tag or sticker.

Records are maintained to identify equipment calibrated, date of calibration, due date for next calibration, NBS certification number for the standards used in calibration and identification of person performing calibration.

External calibration facilities are audited for compliance to MIL-STD-45662.

AUDITS

Compliance to product assurance program systems and operations by Altera, its subcontractors and its vendors is monitored by a documented audit program. This program identifies audit areas, audit schedules, audit check lists, and methods to introduce necessary corrective actions.

VENDOR AND SUBCONTRACTOR AUDITS

The direct material suppliers, assembly subcontractors, environmental and calibration laboratories are audited at least once every year to monitor their compliance to the Product Assurance Program. A major audit discrepancy requires corrective actions on the part of the supplier and a recurring discrepancy results in disqualification.

INTERNAL AUDIT

The Altera manufacturing facility is on a continuous, unannounced self audit system. Quality assurance or its designated representative audit any operation without prior notification. Any discrepancy is recorded on corrective action request form and a response is required from the functional group manager.

PROCESS CONTROL STATISTICS

Manufacturing and Quality ensure that all manufacturing steps are accomplished using documented flow charts, travelers, specifications, approved parts, environmental controls and qualified production equipment.

INCOMING MATERIAL INSPECTION

Incoming material is accepted per applicable quality specifications. The records of inspection results are maintained. Vendor's outgoing quality assurance results are compared with incoming inspection results and any correlation problem is identified and corrected.

PRODUCTION LINE MONITORS AND INSPECTIONS

In-line monitors and inspections include equipment parameter monitors, use of calibration standards, destructive and non-destructive tests to specified limits, proper data recording and use of trend charts.

QUALITY CONTROL - SAMPLING AND INSPECTIONS

All quality control monitors and gates are identified on the flow chart and performed per documented procedures. Sample plans ensure that product quality meets Altera standards and customer requirements. These quality gates and monitors serve two major purposes:

a) Prevent nonconforming products from being shipped to Altera customers.

b) Provide feedback to manufacturing on product quality trends and need for necessary actions.

For military grade products all sampling, inspections and environmental procedures are in accordance with appropriate requirements of MIL-M-38510 and MIL-STD-883.

CONTROL OF NONCONFORMING MATERIALS

The system to control nonconforming materials includes procedures for identification, segregation and disposition of such materials. Altera's system of controlling nonconforming materials covers three distinct areas; nonconforming materials received from suppliers, those detected during manufacturing, and material returned by customers.

RETURN TO VENDOR (RTV)

All nonconforming incoming material which has RTV disposition is segregated. Documentation accompanying such material clearly identifies discrepancy and includes all supporting data. A corrective action response is required from vendors.

MATERIAL REVIEW BOARD (MRB)

The MRB shall consist as a minimum, representatives from Manufacturing, Engineering and Quality Assurance. The MRB is chaired by a representative of Quality Assurance.

The MRB investigates the cause of nonconformance and dispositions the material. Customer and Altera specification requirements are thoroughly reviewed during MRB disposition.

CUSTOMER RETURNS (RMA)

Quality assurance is responsible for coordinating the analysis and disposition of customer returns. Product returned by customers is analyzed in accordance with Altera and customer specifications and necessary corrective actions are initiated.

MANUFACTURING CONTROLS

The sections that follow provide details of key control steps that have been implemented for Altera products. For semiconductor components, the sequence below (Figures 2, 3 and 4) lists the controls for commercial and military ceramic packages as well as plastic packages. These figures provide the details of controls irrespective of whether they are performed by manufacturing or quality control personnel. Every manufacturing step is not necessarily included.

CERAMIC ICs

FIG. 2

COMMERCIAL/INDUSTRIAL

TEST	METHOD (1)	REQUIREMENT
WAFER ELECTRICAL TEST	FULL FUNCTIONAL, VERIFY ERASED PATTERN AND VERIFY ALL BITS	100%
DIE VISUAL (2ND OPTICAL)	2010, CONDITION B	100%
DIE ATTACH MONITOR	DIE SHEAR PER METHOD 2019, X RAY, VISUAL	SAMPLE
BOND STRENGTH MONITOR	2011, CONDITION C	SAMPLE
INTERNAL VISUAL	2010, CONDITION B	100%
SEAL MONITOR	VISUAL, HERMETICITY PER METHODS 1014 B&C.	SAMPLE
STABILIZATION BAKE	METHOD 1008, CONDITION C	100%
TEMPERATURE CYCLE	METHOD 1010, CONDITION C (-65 DEGREE C +150 DEGREE C) 10 CYCLES	100%
LEAD FINISH MONITOR	VISUAL, TIN THICKNESS, SOLDERABILITY	SAMPLE
HERMETICITY	METHOD 1014, CONDITIONS B, C1	100%
FINAL QA ACCEPTANCE AT ASSEMBLY	VISUAL HERMETICITY	SAMPLE

FIG. 2, CONTINUED

TEST	METHOD	REQUIREMENT
INCOMING INSPECTION OF PACKAGES FROM ASSEMBLY	VISUAL, HERMETICITY, LID TORQUE	SAMPLE
PRE-BAKE TEST	ROOM TEMP, FULL FUNCTIONAL, VERIFY ERASED PATTERN, PROGRAM AND VERIFY > 99% OF ALL BITS	100%
EPROM CHARGE (2) RETENTION BAKE	140 DEGREE C, 72 HOURS, N2 AMBIENT	100%
POST BAKE TEST (2)	ROOM TEMP, VERIFY PATTERN, CHECK FOR MARGIN SHIFTING, PROGRAM AND VERIFY REMAINING BITS	100%
PACKAGE PARTS ERASE	ULTRAVIOLET LIGHT	100%
DYNAMIC BURN-IN	125 DEGREE C, 48 HOURS	SAMPLE
POST BURN IN TEST (3)	70 DEGREE C, VERIFY PATTERN, FULL FUNCTIONAL TESTS	100%
TOPSIDE MARK	PART NO, DATE CODE	100%
MARK PERMANENCY	—	SAMPLE
PACKAGE PARTS ERASE	ULTRAVIOLET LIGHT	100%
EXTERNAL VISUAL	METHOD 2009	SAMPLE
FINAL QA ACCEPTANCE	ELECTRICAL, SOLDERABILITY	SAMPLE

(1) ALL METHOD NUMBERS REFERENCED ARE PER MIL-STD-883.

(2) THESE OPERATIONS ARE PERFORMED EITHER AT WAFER OR PACKAGE LEVEL.

(3) FOR INDUSTRIAL/MILITARY TEMPERATURE GRADES APPROPRIATE HOT/COLD TESTING IS PERFORMED.

FIG. 3

MIL-STD-883 CLASS B

TEST	METHOD	REQUIREMENT
WAFER ELECTRICAL TEST	FULL FUNCTIONAL, VERIFY ERASED PATTERN PROGRAM AND VERIFY ALL BITS	100%
DIE VISUAL (2ND OPTICAL)	2010, CONDITION B	100%
DIE ATTACH MONITOR	DIE SHEAR PER METHOD 2019, X RAY, VISUAL	SAMPLE
BOND STRENGTH MONITOR	2011, CONDITION C	SAMPLE
INTERNAL VISUAL	2010, CONDITION B	100%
SEAL MONITOR	VISUAL, HERMETICITY PER METHODS 1014 B&C	SAMPLE
STABILIZATION BAKE	METHOD 1008, CONDITION C (6 HOURS AT 175 DEGREE C)	100%
TEMPERATURE CYCLE	METHOD 1010, CONDITION C (-65 DEGREE C +150 DEGREE C) 10 CYCLES	100%
CONSTANT ACCELERATION	2001, CONDITION E 30kg, Y1 ONLY	100%
LEAD FINISH	PER MIL-M-38510 LEAD FINISH REQUIREMENTS	100%
HERMETICITY	METHOD 1014, CONDITIONS B, C1	100%
FINAL QA ACCEPTANCE AT ASSEMBLY	VISUAL PER METHOD 2009, HERMETICITY PER METHOD 2014	SAMPLE
INCOMING INSPECTION OF PACKAGES FROM ASSEMBLY	VISUAL HERMETICITY, LID TORQUE, TRACEABILITY	SAMPLE
PRE-BAKE TEST	ROOM TEMP, FULL FUNCTIONAL, VERIFY ERASED PATTERN, PROGRAM AND VERIFY > 99% OF ALL BITS	100%
EPROM CHARGE (2) RETENTION BAKE	140 DEGREE C, 72 HOURS, N2 AMBIENT	100%
POST BAKE TEST (2)	ROOM TEMP, VERIFY PATTERN, CHECK FOR MARGIN SHIFTING, PROGRAM AND VERIFY REMAINING BITS	100%

FIG. 3, CONTINUED

MIL-STD-883 CLASS B

TEST	METHOD	REQUIREMENT
PACKAGE PARTS ERASE	ULTRAVIOLET LIGHT	100%
PRE BURN-IN TEST	ROOM TEMP, FULL FUNCTIONAL TEST, VERIFY ERASED PATTERN, PROGRAM AND VERIFY BITS	100%
DYNAMIC BURN-IN	1015, CONDITION D, 125 DEGREES C, 160 HOURS MIN.	100%
POST BURN IN TEST	A. ROOM TEMP, VERIFY PATTERN, STATIC TESTS PDA $\leq$ 5%	100%
	B. ROOM TEMP, VERIFY PATTERN, FULL FUNCTIONAL TEST	100%
GROUP A	ROOM TEMP	LTPD 2%
POST BURN IN TEST	125 DEGREES C	100%
GROUP A	125 DEGREES C	LTPD 3%
POST BURN IN TEST	-55 DEGREES C	100%
GROUP A	-55 DEGREES C	LTPD 3%
TOPSIDE MARK	PART NO, DATE CODE	100%
PACKAGE PART ERASE	ULTRAVIOLET LIGHT	100%
EXTERNAL VISUAL	METHOD 2009	100%
FINAL QA ACCEPTANCE	GROUP B PER METHOD 5005.8 AND REQUIREMENTS OF MIL-M-38510	ALL LOTS

(1) ALL METHOD NUMBERS ARE REFERENCED PER MIL-STD-883.

(2) THESE OPERATIONS ARE PERFORMED EITHER AT WAFER OR PACKAGE LEVEL.

NOTE: GROUP C AND GROUP D TESTS ARE PERFORMED ON QUALIFICATION LOTS AND PER QCI REQUIREMENTS OF MIL-STD-883.

FIG. 4

COMMERCIAL/INDUSTRIAL

TEST	METHOD/CONDITION (1)	REQUIREMENT
WAFER FUNCTIONAL TEST	FULL FUNCTIONAL, VERIFY ERASED PATTERN PROGRAM AND VERIFY > 99% OF BITS	100%
EPROM CHARGE RETENTION BAKE	140 DEG C, 72 HOURS N2 AMBIENT	100%
POST BAKE WAFER TEST	VERIFY PATTERN, CHECK FOR MARGIN SHIFTING, PROGRAM AND VERIFY REMAINING BITS	100%
DIE VISUAL	ALTERA SPECIFICATION	100%
DIE ATTACH MONITOR	DIE SHEAR, VISUAL	SAMPLE
BOND STRENGTH MONITOR	METHOD 2011, CONDITION C	SAMPLE
INTERNAL VISUAL	30X, MAGNIFICATION	100%
MOLD MONITOR	MOLD COMPOUND INSPECTION, VISUAL INSPECTION OF PACKAGES, X RAY MONITOR FOR WIRE SWEEP	SAMPLE
MOLD CURE	150 DEGREE C, 8 HOURS	100%
LEAD FINISH MONITOR	SOLDERABILITY, VISUAL	100%
OPEN-SHORT TEST	OHMIC CONTINUITY	SAMPLE
FINAL QA ACCEPTANCE AT ASSEMBLY	VISUAL	SAMPLE
INCOMING INSPECTION OF PACKAGES FROM ASSEMBLY	VISUAL, TRACEABILITY	SAMPLE
PRE BURN-IN ELECTRICAL	ALTERA ELECTRICAL TEST PROGRAM	100%
DYNAMIC BURN-IN	125 DEGREE C, 48 HOURS	SAMPLE
FINAL TEST	ALTERA ELECTRICAL TEST PROGRAM	100%
TOPSIDE MARK	PART NO, DATE CODE	100%
MARK PERMANENCY	—	SAMPLE
PACKAGE PARTS ERASE	ULTRAVIOLET LIGHT	100%
EXTERNAL VISUAL	ALTERA SPEC.	SAMPLE
FINAL QA ACCEPTANCE	ELECTRICAL, SOLDERABILITY	SAMPLE

(1) ALL METHOD NUMBERS REFERENCED ARE PER MIL-STD-883.

ELECTRICAL CHARACTERIZATION

Before being released for production, Altera components undergo exhaustive characterization tests performed on both bench setups and automatic testers. The purpose of these tests is not only to verify data sheet performance, but to seek out any operating weaknesses that could affect even a small fraction of applications.

All Altera components are characterized over the full military temperature range of -55°C to +125°C. Supply voltage range of at least 4.25-5.75 volts are characterized. Both AC and DC data sheet parameters are characterized. In addition, a sensitivity analysis is performed which monitors functionality and speed performance over the broadest possible range of data pattern, choice of input and output pins, input waveform slope, and power supply transients.

TEST PHILOSOPHY

The EPROM technology employed in Altera products allows reprogrammability. In conjunction with careful design techniques, this provides complete generic testability. 100% testing is a fundamental part of Altera's test philosophy. All EPROM bits and all features of each part are tested as part of the standard production flow. Even in the case of plastic packaged one-time-programmable (OTP) components, special test features allow complete coverage with the combination of die level and packaged part tests.

LIFE TEST

As part of the qualification of each product, life testing at 125°C under dynamic operating conditions is performed. This life test extends to 2000 hours.

HIGH TEMPERATURE BAKE

In addition to the dynamic life tests, EPROM cell reliability is qualified through retention testing to 1000 hours at 140°C.

ESD

All Altera components are thoroughly tested for electrostatic discharge (ESD) sensitivity prior to their release for production. All pins are tested with procedures which match or exceed the technique of method 3015.2 of MIL-STD-883.

LATCH UP

Standardized latch up tests are performed on all input and output pins of each product as part of its characterization prior to production release. These tests employ industry accepted methods of subjecting the product to unusual current and voltage conditions at its pins.

PACKAGE QUALIFICATION TESTS

Package integrity tests are performed for all new packages, assembly plants, process, material and equipment changes. The selection of qualification tests depends on the change to be qualified. For a totally new package and assembly plant, a series of qualification tests are performed to ensure that the package quality and reliability meet Altera standards of mechanical integrity and cosmetic finish.

For material, process or equipment changes, only selected tests are performed depending on the type of changes.

Product Reliability program is described in figure 6.

HARDWARE IMPLEMENTATION PROCEDURE

For the development hardware products offered by Altera, any modification of hardware has a direct impact on existing software as well as the integrated circuits that are supported by the subject hardware. It is therefore essential that hardware be qualified with the applicable versions of Software and integrated circuits. New hardware implementation requires successful completion of the sequence of tests are listed in Figure 5, before its release to end users.

Testing is performed for each of the integrated circuit device types as follows:

Full programming

Functional test on automatic test equipment used for normal production ELPD testing

Complement pattern testing of the prior tests

Circuit tests performed ensure "blank check," "program/verify" and "examine/re-verify."

The procedure below ensures that any incompatibility between the new and existing hardware, software & integrated circuits is detected at Altera and results in required corrective actions.

FIG. 5

Test Step Description	Performed by
Full electrical & functional testing of prototype hardware	Development Engineering
Functional testing with software & samples of applicable UCIC products	Development Engineering
Regression testing as required	Development Engineering
Acceptance testing as follows:	
Current production release of software	Product Engineering & Quality Assurance
Current production release of other unchanged hardware	Product Engineering & Quality Assurance
Multiple sets of new hardware	Product Engineering & Quality Assurance
Multiple samples of each of the EPLD device types	Product Engineering & Quality Assurance

PRODUCT DOCUMENTATION

PHILOSOPHY

Altera employs extensive formal product documentation aimed at ensuring the broadest possible access within the company to key product information, while maintaining an accurate historical record. This documentation can be grouped into three categories.

1. Engineering Documentation—key product information that describes in detail the product design, characterization results, and test programs.
2. Production Documentation—includes documentation of all production procedures, maintenance, and test hardware tools.
3. Change Control Documentation—is the detailed history of evolutionary improvements in product design or testing tools.

SOFTWARE METHODOLOGY

Every Altera software product is subjected to a rigorous set of both automatic and manual (interaction) test procedures before it is qualified for release to production.

There are three stages of testing:

A. Engineering tests
B. Alpha site tests
C. Beta site tests

The goals of these tests are (1) to ensure that the software performs according to the specification and (2) to guarantee that modifications have not introduced new errors to a previously qualified version of the software.

ENGINEERING TESTS

These tests are performed by Software Design Engineering and Software Product Engineering. There are two categories of tests: Enhancement Tests and Regression Tests. A test or a series of tests are designed to check for correct operation of an enhancement or a new function added to a software product. A new version of the software product must pass all the Enhancement Tests before going to the Regression Testing.

Regression Tests are a collection of all the tests that have been used to qualify the product at its previous version. Once an Enhancement Test is checked out, it is added to the Regression Test set. Any time any change is made to a software product, however small, the software is subjected to Regression Testing procedure.

ALPHA SITE TESTS

These tests are performed in the IC Design and Applications Engineering departments. The goal of these tests is to check the functionality of the software in an approximate end user application environment, and to reduce the potential for errors in the final Beta testing.

BETA SITE TESTS

These tests are performed by Altera Applications engineering and selected customers. In addition to checking the correct functionality of the software, these tests are used as a vehicle for collecting improvements and enhancements to the product. The major difference in procedure between the Alpha and Beta testing is that in the latter, the test site has very little interaction with the software engineering department during testing.

SOFTWARE PROBLEM REPORT (SPR) AND TRACKING

Every time an error is detected in any of the above stages of testing, a SPR is generated. These SPRs are tracked for resolution of problems as well as for updating the Regression Tests to catch the error in the future.

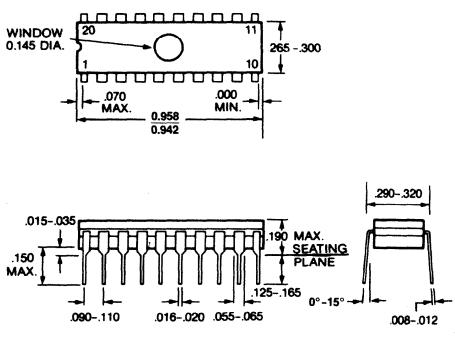
RELIABILITY TEST PROGRAM

FIG. 6

TYPE OF TEST	MIL-STD-883 METHOD/CONDITION	FREQUENCY	PLASTIC	HERMETIC
Temperature Cycling	1010C, -65°C to +150°C, 100 cycles	Qualification, 2x/year per package	X	X
Thermal Shock	1011B, -55°C to +125°C, 100 cycles	Qualification, 2x/year per package	—	X
Mechanical Shock	2002B, 1500g force, .5ms pulse peak	Qualification, 2x/year per package	—	X
Constant Acceleration	2001E, 30,000g force, Y1 only	Qualification, 2x/year per package	—	X
Lid Torque	2024	Qualification, 1x/month per package	—	X
Lead Fatigue	2004 B2	Qualification, 1x/quarter per package	—	X
Internal Water Vapor	1018, 5000 ppm max at 100°C	Qualification, 1x/quarter per sealing process	—	X
Biased Humidity/ Temp. test	85°C, 85% R.H. 1000 hours min.	Qualification, 2x/year per plastic process	X	—
Pressure Cooker Test	121°C, 15PSIG 96 hrs. min.	Qualification, 1x/month per plastic process	X	—
Life Test	1000 hours at 125°C at rated voltages	Qualification, 1x/quarter per device	X	X
Retention Bake	1000 hours min. at 140°C	Qualification, 2x/year per process	X	X

Package Type	Package-Code	Lead Material	Lead Finish
Plastic Dual-in-line	P	Copper	Solder dip (60/40)
Plastic Chip carrier	L	Copper	Solder plate (60/40)
Ceramic Dual-in-line	D	Alloy 42	Solder-Dip over tin flash (Military) Matte Tin plate
Ceramic Chip carrier	J	Alloy 42	Solder dip (60/40)
Pin-Grid-Array	G	Alloy 42	Gold over Nickel plate

20 PIN DIP CERAMIC



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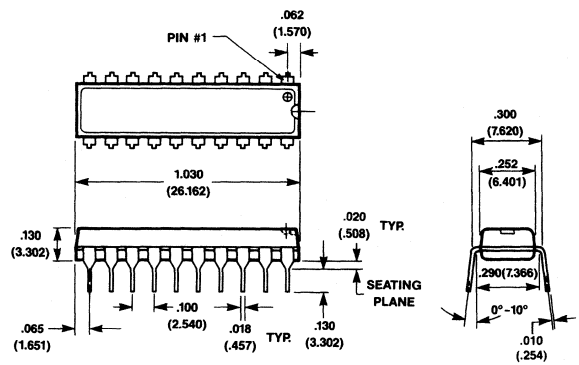

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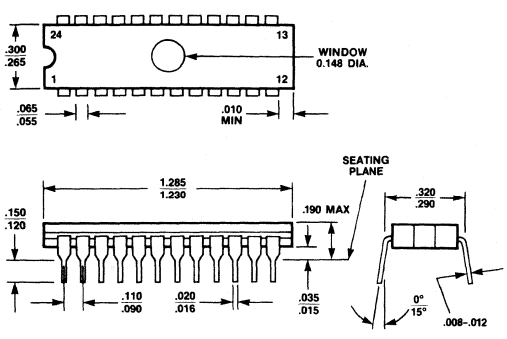

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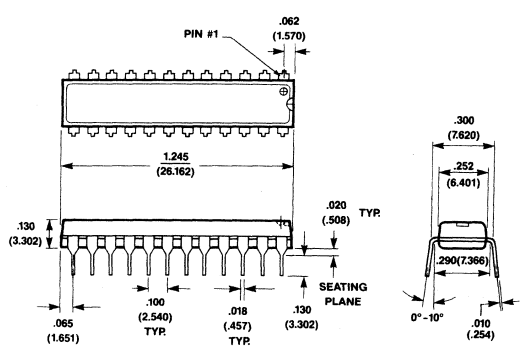

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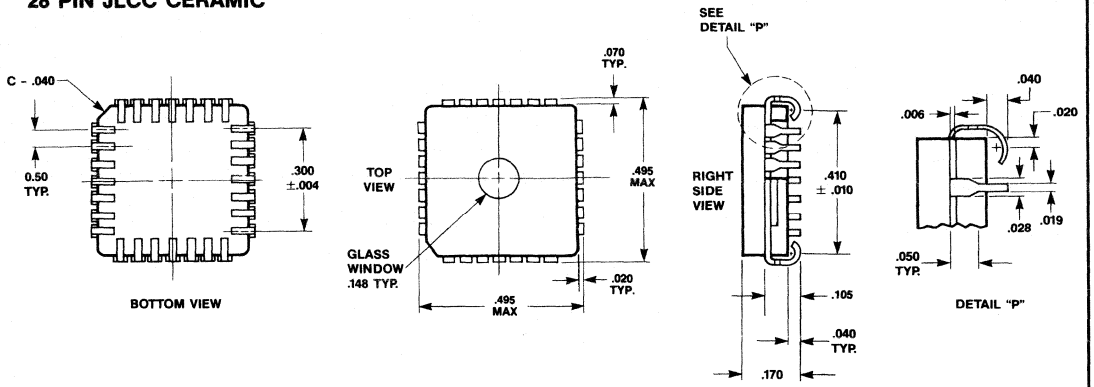

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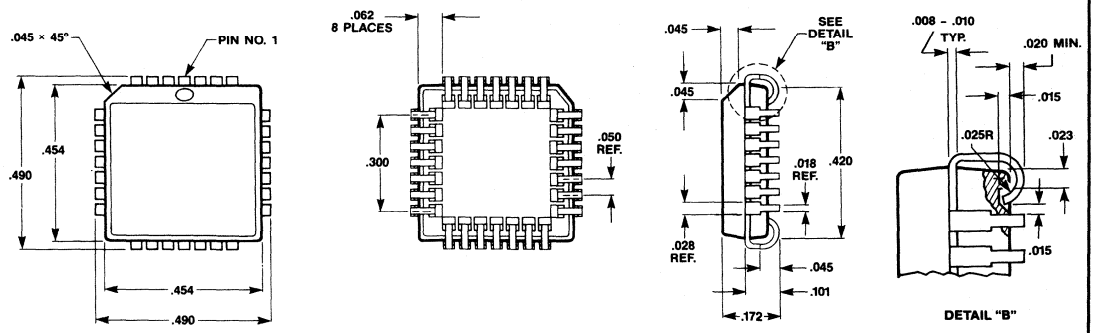

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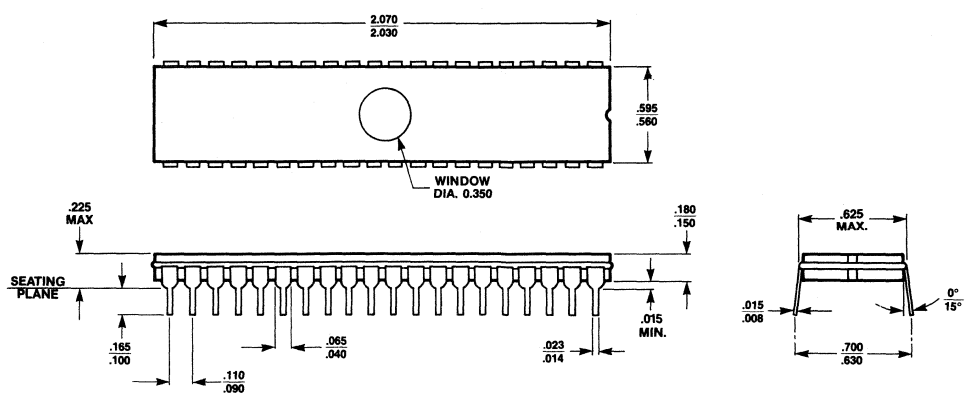

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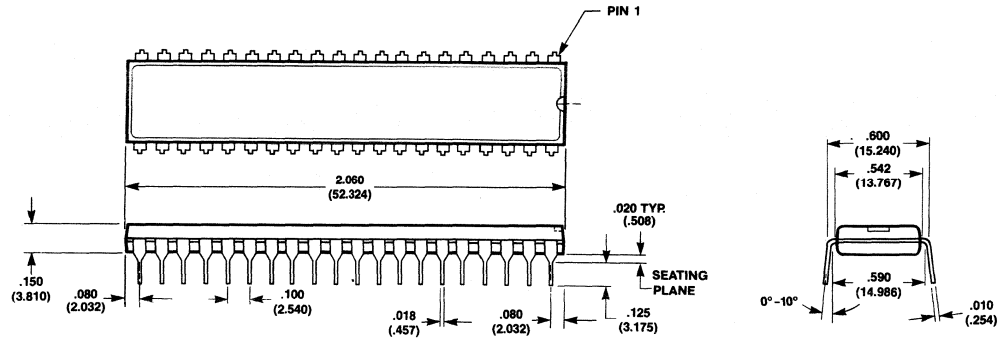

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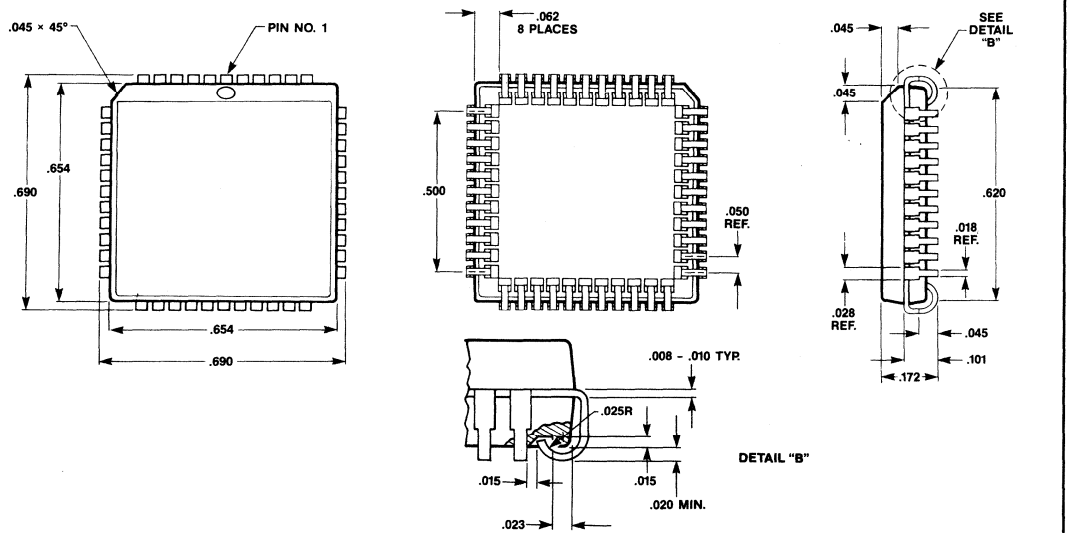

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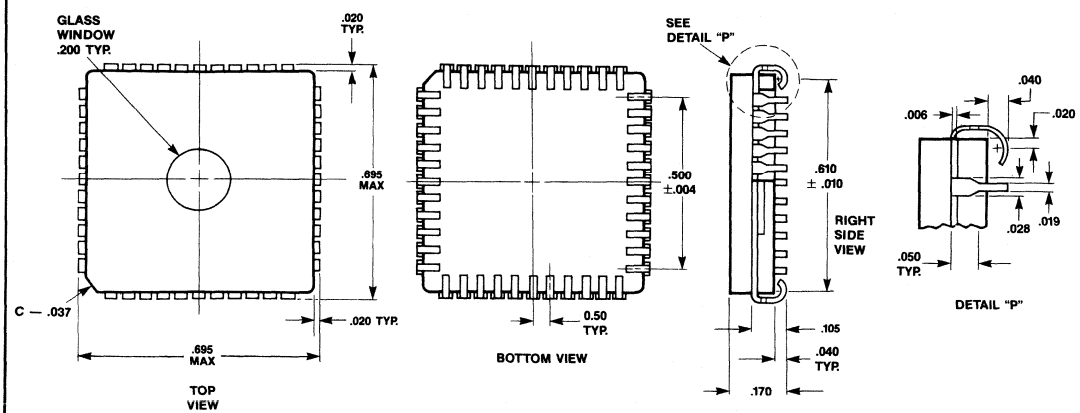

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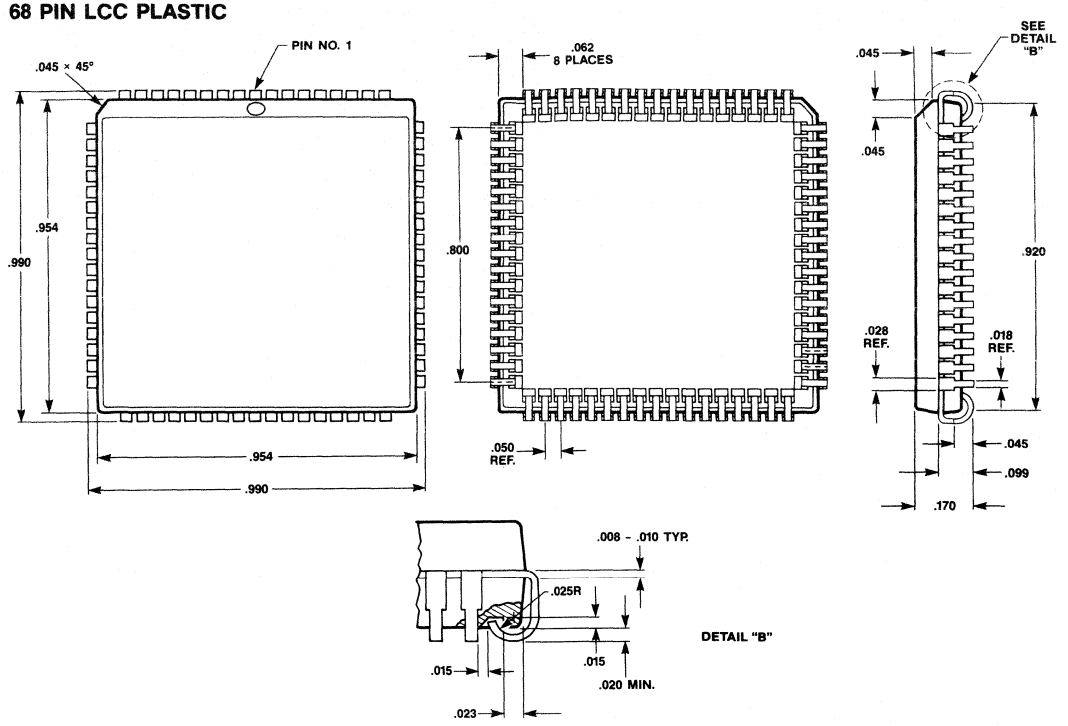

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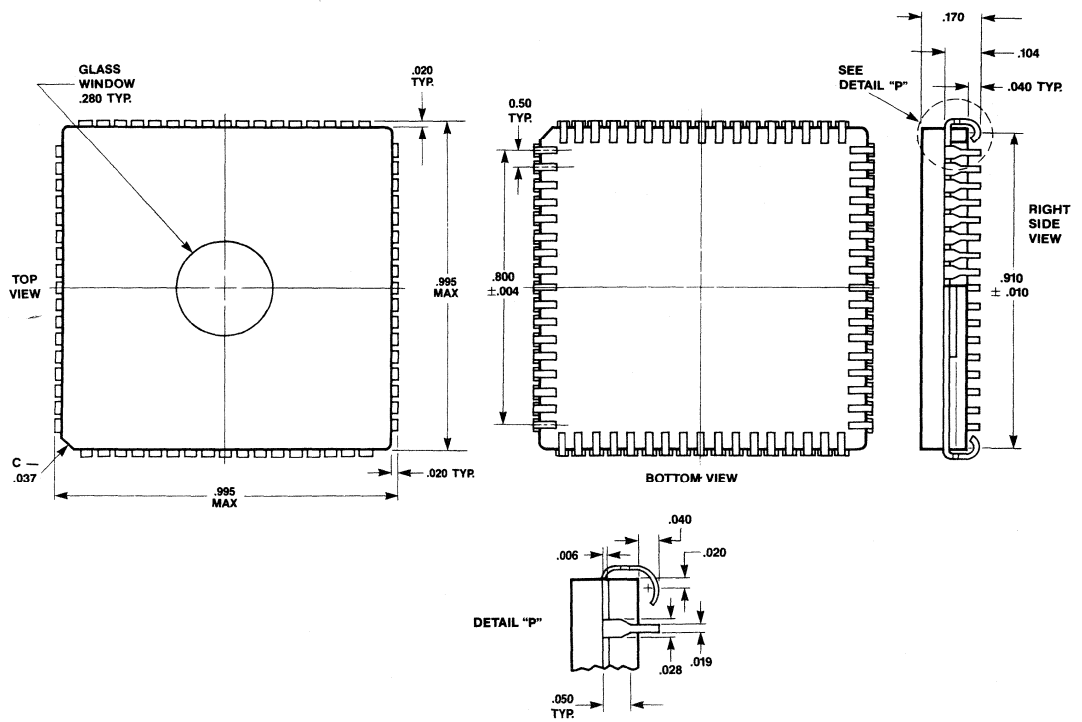

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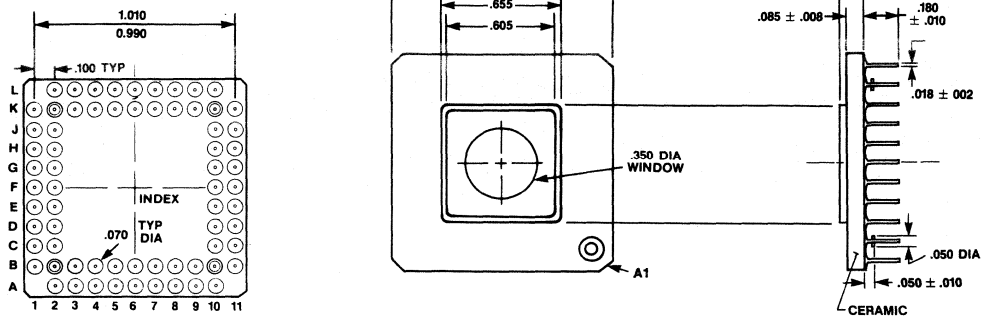
68 PIN PGA CERAMIC



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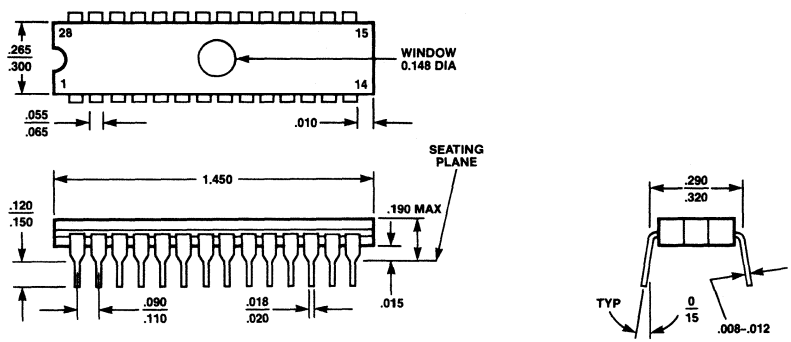

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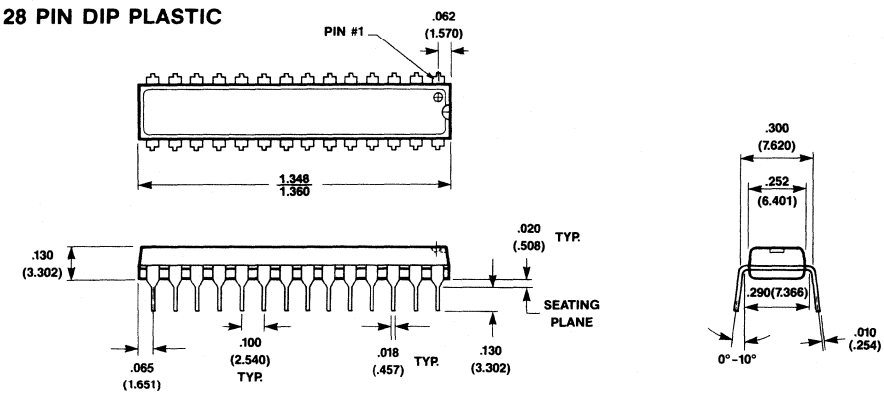

THERMAL RESISTANCE (°C/W)

Pin No.	Package	θ_{JA}	θ_{JC}	θ_{CA}
20	CERDIP	62	17	45
20	PDIP	48	14	34
24	CERDIP	64	8	56
24	PDIP	64	11	53
28	CERDIP	52	24	28
28	PDIP	62	40	22
28	JLCC	72	16	56
28	PLCC	57	17	40
40	CERDIP	40	7	33
40	PDIP	46	19	27
44	JLCC	68	16	52
44	PLCC	49	14	35
68	JLCC	47	7	40
68	PLCC	41	15	26
68	PGA	43	5	38

Notes:

1. All Thermal Characteristics are measured using the TSP (Temperature Sensitive Parameter) test method described in MIL STD 883C, Method 1012.1.
2. The formula for determining θ_{JX} is $\theta_{JX} = (T_J - T_A)/PD$ where T_J = die junction temperature, T_A = ambient temperature and P_D = power being dissipated in the device causing a temperature rise at the die junction. T_J is determined by characterizing the relationship between the forward biased voltage and temperature of the isolation diode between the power and ground pins of the IC.
3. All thermal resistance values measured with package soldered into PC boards excluding 24 pin CERDIP and PDIP which was socket mounted.
4. All thermal resistance values accurate to ±5 °C/W.

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